M.E. Degree

in

APPLIED ELECTRONICS

CURRICULUM & SYLLABUS (CBCS)

(For students admitted from the Academic Year 2022-2023)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

St. XAVIER'S CATHOLIC COLLEGE OF ENGINEERING

CHUNKANKADAI, NAGERCOIL – 629 003.

KANYAKUMARI DISTRICT, TAMIL NADU, INDIA

St. XAVIER'S CATHOLIC COLLEGE OF ENGINEERING

CHUNKANKADAI, NAGERCOIL – 629 003.

AUTONOMOUS COLLEGE AFFILIATED TO ANNA UNIVERSITY

ACADEMIC REGULATIONS 2022

M.E. APPLIED ELECTRONICS CURRICULUM

CHOICE BASED CREDIT SYSTEM

Inconsonance to the vision of our College,

An engineering graduate we form would be a person with optimal human development, i.e. physical, mental, emotional, social and spiritual spheres of personality.

He/she would be also a person mature in relationships, especially knowing how to treat everyone with respect, including persons of complementary gender with equality and gender sensitivity guided by clear and pro-social values.

He would be patriotic and would hold the Indian Constitution and all the precepts it outlays close to his heart and would have a secular spirit committed to safeguard and cherish the multi-cultural, multi- religious and multi-linguistic ethos of Indian Society.

Academically, he/she would be a graduate with a strong engineering foundation with proficient technical knowledge and skills. He would have enough exposure and experience into the ethos of relevant industry and be industry ready to construct a successful career for himself and for the benefit of the society.

He would have been well trained in research methodology and would have established himself as a researcher having taken up many research projects, with sound ethical standards and social relevance. He would be a person with a passion for technical innovations committed to lifelong learning and research.

He would be well prepared and confident to develop ingenuous solutions to the problems people face as an individual and as a team and work for the emancipation of our society with leadership and courage.

M.E Applied Electronics is a post-graduate program that combines engineering knowledge and practical application to address real-world problems. This program is offered to provide a broad knowledge and practical experience in Applied Electronics with fundamentals and cutting-edge technology in electronic system design , signal & image processing , semiconductor devices modelling and design, Analog & Digital IC design. The course offers the basic skills, in relation to recent techniques in electronic design and processing analog and digital signals acquired from sensors and actuators. The course provides study of technological processes as base of the CMOS digital integrated circuits. The course also provides skills to design and test relatively complex digital architectures through the use of VHDL. It is designed to help graduates develop ethical and moral values while learning to design, implement, and manage electronics systems for societal needs.

I. PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

I	Teach students to acquire knowledge in latest hardware and software required for designing and critically analyzing electronic circuits related to industry and society.
II	Motivate students to propose innovative solutions for socially significant and challenging projects, for societal benefits.
III	To enable the graduates to adapt to advancements in technology through self-learning and to pursue research to meet out the demands in industries and Academia.
IV	Mould students to progress and develop with ethics, leadership skills and to communicate effectively.
V	To motivate students to become entrepreneurs to develop indigenous solutions.

II. PROGRAMME OUTCOMES (POs)

PO	Programme Outcomes
1	Independently carry out research/investigation and development work to solve practical problems.
2	Write and present substantial technical report/document.
3	Demonstrate a degree of mastery over the electronic system design at a level higher than the requirements in the appropriate bachelor program
4	To evaluate the design and provide optimal solutions to problems in advanced signal processing, digital system design, embedded systems, Internet of things and VLSI design
5	To develop electronic systems using latest engineering hardware and software tools.
6	To work professionally and ethically, adapt to technological changes, communicate effectively, work and lead a team and practice responsibly in a global environment in the area of applied electronics

PEO's – PO's & PSO's MAPPING

PROGRAMME EDUCATIONAL OBJECTIVES	PROGRAMME OUTCOMES					
	1	**2**	**3**	**4**	**5**	**6**
I	**1**	**3**	**1**	**2**	**-**	**-**
II	**2**	**-**	**1**	**2**	**-**	**2**
III	**2**	**-**	**-**	**1**	**1**	**2**
IV	**-**	**-**	**1**	**-**	**-**	**1**
V	**1**	**-**	**1**	**2**	**1**	**-**

PROGRAMME ARTICULATION MATRIX

Year	Semester	Course Name	PO					
			1	2	3	4	5	6
I	I	Applied Mathematics for Electronics Engineers	2	2	-	-	-	1
		Digital CMOS VLSI Design	1	-	1	2	-	-
		Advanced Digital System Design	2	1	1	1	1	1
		Electronics System Design Laboratory	1.6	1	1.8	3	1.5	2
I	II	Power Conversion Circuits for Electronics	2	1	2	1	1	1
		Semiconductor Devices and Modeling	2	1	2	1	1.4	1.4
		Advanced Digital Signal Processing	2	1	2	2	2	1
		Embedded Systems	2	-	2	1	2	1
		VLSI Design Laboratory	1.6	1	1.8	2	1.5	2

M.E. APPLIED ELECTRONICS CURRICULUM

SEMESTER I

SL. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY COURSES								
1.	MA22103	Applied Mathematics for Electronics Engineers	FC	3	1	0	4	4
2.	AE22102	Digital CMOS VLSI Design	PCC	3	0	0	3	3
3.		Professional Elective - I	PEC	3	0	0	3	3
THEORY COURSES WITH PRACTICAL COMPONENT								
4.	AE22101	Advanced Digital System Design	PCC	3	0	2	5	4
PRACTICAL COURSES								
5.	AE22103	Electronics System Design Laboratory	PCC	0	0	4	4	2
EMPLOYABILITY ENHANCEMENT COURSES								
6.	AE22104	Technical Seminar	EEC	0	0	2	2	1
7.	RM22101	Research Methodology	RMC	2	0	0	2	2
MANDATORY COURSES								
8.		Audit Course – I	AC	2	0	0	2	0
TOTAL				**16**	**1**	**8**	**25**	**19**

SEMESTER II

SL. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY COURSES								
1.	AE22204	Power Conversion Circuits for Electronics	PCC	3	0	0	3	3
2.		Professional Elective II	PEC	3	0	0	3	3
3.		Professional Elective III	PEC	3	0	0	3	3
THEORY COURSES WITH PRACTICAL COMPONENT								
4.	AE22201	Semiconductor Devices and Modeling	PCC	3	0	2	5	4
5.	AE22202	Advanced Digital Signal Processing	PCC	3	0	2	5	4
6.	AE22203	Embedded Systems	PCC	3	0	2	5	4
PRACTICAL COURSES								
7.	AE22205	VLSI Design Laboratory	PCC	0	0	4	4	2
EMPLOYABILITY ENHANCEMENT COURSES								
8.	RM22201	Research Tools Laboratory	RMC	0	0	4	4	2
MANDATORY COURSES								
9.		Audit Course – II	AC	2	0	0	2	0
TOTAL				**20**	**0**	**14**	**34**	**25**

SEMESTER III

SL. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY COURSES								
1.		Professional Elective V	PEC	3	0	0	3	3
2.		Open Elective	OEC	3	0	0	3	3
THEORY COURSES WITH PRACTICAL COMPONENT								
3.		Professional Elective IV	PEC	3	0	2	5	4
EMPLOYABILITY ENHANCEMENT COURSES								
4.	AE22301	Inplant / Industrial / Practical Training (4 weeks during summer vacation)	EEC	0	0	4	4	2
5.	AE22302	Project Work I	EEC	0	0	6	6	3
TOTAL				**9**	**0**	**12**	**21**	**15**

SEMESTER IV

SL. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
EMPLOYABILITY ENHANCEMENT COURSES								
1.	AE22401	Project Work II	EEC	0	0	24	24	12
TOTAL				**0**	**0**	**24**	**24**	**12**

TOTAL CREDITS: 71

LIST OF PROFESSIONAL ELECTIVE COURSES (PEC)

SEMESTER I, PROFESSIONAL ELECTIVE I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	AE22111	Applications Specific Integrated Circuits	PEC	3	0	0	3	3
2.	AE22112	Electromagnetic Interference and Compatibility	PEC	3	0	0	3	3
3.	AE22113	Analog and Mixed Signal IC Design	PEC	3	0	0	3	3
4.	AE22114	VLSI Testing	PEC	3	0	0	3	3
5.	AE22115	Soft Computing and Optimization Techniques	PEC	3	0	0	3	3

SEMESTER II, PROFESSIONAL ELECTIVE II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	CU22322	RF System Design	PEC	3	0	0	3	3
2.	AE22211	Robotics	PEC	3	0	0	3	3
3.	AE22212	Computer Architecture and Parallel Processing	PEC	3	0	0	3	3
4.	AE22213	VLSI Design Techniques	PEC	3	0	0	3	3
5.	AE22214	Industrial Internet of Things	PEC	3	0	0	3	3

SEMESTER II, PROFESSIONAL ELECTIVE III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	AE22221	Quantum Computing	PEC	3	0	0	3	3
2.	CU22222	VLSI for Wireless Communication	PEC	3	0	0	3	3

3.	AE22222	Micro Electro Mechanical Systems	PEC	3	0	0	3	3
4.	AE22223	CAD for VLSI Circuits	PEC	3	0	0	3	3
5.	AE22224	Hardware Secure Computing	PEC	3	0	0	3	3

SEMESTER III, PROFESSIONAL ELECTIVE IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	AE22311	Modeling and Synthesis with HDL	PEC	3	0	2	5	4
2.	MX22313	Deep Learning	PEC	3	0	2	5	4
3.	AE22312	Digital Image Processing	PEC	3	0	2	5	4
4.	MX22203	Machine Learning Techniques	PEC	3	0	2	5	4
5.	AE22313	PCB Design	PEC	3	0	2	5	4

SEMESTER III, PROFESSIONAL ELECTIVE V

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	AE22321	Sensors and Actuators	PEC	3	0	0	3	3
2.	AE22322	Digital High Speed Design	PEC	3	0	0	3	3
3.	AE22323	Consumer Electronics	PEC	3	0	0	3	3
4.	AE22324	Advanced Microprocessors and Microcontrollers Architecture	PEC	3	0	0	3	3
5.	AE22325	Automotive Electronics	PEC	3	0	0	3	3

AUDIT COURSES (AC)

SL. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	AC22101	English for Research Paper Writing	AC	2	0	0	2	0
2.	AC22102	Constitution of India	AC	2	0	0	2	0
3.	AC22201	Disaster Management	AC	2	0	0	2	0
4.	AC22202	நற்றமிழ் இலக்கியம	AC	2	0	0	2	0

LIST OF OPEN ELECTIVES

SL. NO.	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
			L	T	P		
1.	PE22354	Smart Grid	3	0	0	3	3

2.	SE22351	Structural Health Monitoring	3	0	0	3	3
3.	SE22341	Smart Materials and Smart Structures	3	0	0	3	3
4.	CP22351	Agile Methodologies	3	0	0	3	3
5.	CP22344	Data Visualization Techniques	3	0	0	3	3

SUMMARY

M.E. Applied Electronics						
S. No.	**Subject Area**	**Credits per Semester**				**Total Credits**
		I	**II**	**III**	**IV**	
1	**FC**	**4**	**-**	**-**	**-**	**4**
2	**PCC**	**9**	**17**	**-**	**-**	**26**
3	**PEC**	**3**	**6**	**7**	**-**	**16**
4	**OEC**	**-**	**-**	**3**	**-**	**3**
5	**EEC**	**1**	**-**	**5**	**12**	**18**
6	**RMC**	**2**	**2**	**-**	**-**	**4**
7	**Non-Credit AC**	**0**	**0**	**-**	**-**	**0**
TOTAL		**19**	**25**	**15**	**12**	**71**

SEMESTER I

MA22103	**APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS**	**L**	**T**	**P**	**C**
		3	**1**	**0**	**4**

COURSE OBJECTIVES:

- To understand the basics of random variables with emphasis on the standard discrete and continuous distributions
- To understand the basic probability concepts with respect to two dimensional random variables
- To make students understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete – time Markov chains
- To provide the required fundamental concepts in queuing models and apply these techniques in networks, image processing

UNIT I	**FUZZY LOGIC**	**12**

Classical logic – Logic functions of two variables – Properties of Boolean algebras – Multivalued logics – Primitives of some three-valued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II	**PROBABILITY AND RANDOM VARIABLES**	**12**

Probability - Axioms of probability - Conditional probability - Baye's theorem- Discrete random variable – Probability mass function– Continuous random variable – Probability density function – Properties - mean, variance – Special distributions: Binomial, Poisson and Normal distributions (Derivations not included).

UNIT III	**TWO DIMENSIONAL RANDOM VARIABLES**	**12**

Two dimensional Random variables-Discrete and continuous Joint distributions –Discrete and continuous Marginal distributions - conditional distributions - Central limit theorem(excluding proof) –Covariance-– Correlation –Karl Pearson correlation coefficient-Regression- Regression lines-Regression coefficient.

UNIT IV	RANDOM PROCESSES	12
Classification – Stationary random process – Markov process – Markov chain – Poisson process - Discrete parameter Markov chain - Chapman Kolmogorov equations (Statement only) - Limiting distributions – Auto correlation – Cross correlation.		
UNIT V	**QUEUEING MODELS**	**12**
Elements of queuing system – Kendall's notation - Markovian queues – Single channel queueing model - multi channel queuing model – Little's formula – Steady state analysis – Self-service queue.		
		TOTAL: 60 PERIODS

COURSE OUTCOMES:	
At the end of the course, the students will be able to:	
CO1:	Define fuzzy logic, probability, random processes and queuing models
CO2:	Classify fuzzy, distributions, and random processes
CO3:	Explain the ideas of single and multiple server queueing models
CO4:	Apply Fuzzy prepositions, random variables, Markov and Poisson processes in electronics field
CO5:	Apply queuing models with finite and infinite capacity to solve practical problems

REFERENCES:

1.	Dallas E Johnson, "Applied multivariate methods for data Analysis", Thomson and Duxbury press, Singapore, 1998.
2.	Richard A. Johnson and Dean W. Wichern, "Applied multivariate statistical Analysis", Pearson Education, 6th Edition, New Delhi, 2023.
3.	S.P.Gupta, "Statistical Methods", Sultan Chand & Sons, 48th edition, New Delhi, 2022.
4.	Oliver C. Ibe, "Fundamentals of Applied probability and Random Processes", Academic Press, Boston, 2014.
5.	Johnson R. A. and Gupta C.B., "Miller and Freund's Probability and Statistics for Engineers", Pearson India Education, Asia, 9th Edition, New Delhi, 2017. Jersey, 2004.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	2	-	-	-	-
CO2	2	2	-	-	-	-
CO3	2	2	-	-	-	1
CO4	2	2	-	-	-	1
CO5	2	2	-	-	-	1
CO	2	2	-	-	-	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qns.	Total 16 Marks Qns.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse (An) Evaluate (Ev)
Unit-I: FUZZY LOGIC	2	1 either or	1(2)-CO1	1(2)-CO2	1either or (16)-CO4	-
Unit-II: PROBABILITY AND RANDOM VARIABLES	2	1 either or	1(2)-CO1	1(2)-CO2	1either or (16)-CO4	-

Unit-III: TWO DIMENSIONAL RANDOM VARIABLES	2	1 either or	1(2)-CO1	1(2)-CO2	1either or (16)-CO4	-
Unit-IV: RANDOM PROCESSES	2	1 either or	1(2)-CO1	1(2)-CO2	1either or (16)-CO4	-
Unit-V: QUEUEING MODELS	2	1 either or	1(2)-CO1	1(2)-CO3	1either or (16)-CO5	-
Total Qns.	10	5 either or	5(2)	5(2)	5 either or (16)	-
Total Marks	20	80	10	10	80	-
Weightage	20%	80%	10%	10%	80%	-

Weightage for COs

	CO1	**CO2**	**CO3**	**CO4**	**CO5**
Total Marks	10	8	2	64	16
Weightage	10%	8%	2%	64%	16%

AE22102	**DIGITAL CMOS VLSI DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To introduce the transistor level design of all digital building blocks common to all CMOS microprocessors, network processors, digital backend of all wireless systems etc.
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption

UNIT I	**MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER**	**12**

MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, elmore constant, CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters.

UNIT II	**COMBINATIONAL LOGIC CIRCUITS**	**9**

Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates.

UNIT III	**SEQUENTIAL LOGIC CIRCUITS**	**9**

Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, non bistable sequential circuits. Interconnect and Clocking Strategies.

UNIT IV	**ARITHMETIC BUILDING BLOCKS**	**9**

Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.

UNIT V	**MEMORY ARCHITECTURES**	**6**

Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read- Write Memories (RAM), dynamic memory design, Transistor SRAM cell, sense amplifiers.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Describe basics of CMOS digital integrated circuits
CO2:	Describe the memory process for VLSI circuits

CO3:	Construct the design methodology of memory architectures and arithmetic building blocks
CO4:	Analyze combinational and sequential logic circuits
CO5:	Design and analyze digital CMOS circuits

REFERENCES:

1.	N.Weste, K. Eshraghian, " Principles of CMOS VLSI Design", Addision Wesley, 2nd Edition, 1993
2.	M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
3.	Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design", Mcgraw-Hill, Revised 4th Edition, 2019.
4.	Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective", Prentice Hall Of India, 2nd Edition, 2016
5.	Neil H.E.Weste, David Money Harris, "CMOS VLSI Design-A Circuit and Systems Perspective", Pearson, 4th Edition, 2015.
6.	R. Jacob Baker , "CMOS: Circuit Design, Layout, and Simulation", 4th Edition, Wiley-IEEE Press, 2019.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	-	1	2	-	-
CO2	1	-	1	2	-	-
CO3	1	-	1	2	-	-
CO4	1	-	1	2	-	-
CO5	1	-	1	2	-	-
CO	1	-	1	2	-	-

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I:MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: COMBINATIONAL LOGIC CIRCUITS	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: SEQUENTIAL LOGIC CIRCUITS	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV:. ARITHMETIC BUILDING BLOCKS	2	1either or	1(2)-CO3	1(2)-CO3	1either or (16)-CO4	-
Unit-V: MEMORY ARCHITECTURES	2	1either or	1(2)-CO3	1(2)-CO5 1either or		-

				(16)-CO5		
Total Qns. Title: AE22102-DIGITAL CMOS VLSI DESIGN	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22101	**ADVANCED DIGITAL SYSTEM DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To design asynchronous sequential circuits
- To learn about hazards in asynchronous sequential circuits
- To study the fault testing procedure for digital circuits
- To understand the architecture of programmable devices
- To design and implement digital circuits using programming tools

UNIT I **SEQUENTIAL CIRCUIT DESIGN** **9**

Analysis of Clocked Synchronous Sequential Circuits and Modeling - State Diagram, State Table, State Table Assignment and Reduction-Design of Synchronous Sequential Circuits Design of Iterative Circuits-ASM Chart and Realization using ASM

UNIT II **ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN** **9**

Analysis of Asynchronous Sequential Circuit – Flow Table Reduction-Races-State Assignment-Transition Table and Problems in Transition Table- Design of Asynchronous Sequential Circuit - Static, Dynamic and Essential hazards — Mixed Operating Mode Asynchronous Circuits — Designing Vending Machine Controller.

UNIT III **FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS** **9**

Fault Table Method-Path Sensitization Method – Boolean Difference Method - D Algorithm — Tolerance Techniques – The Compact Algorithm – Fault in PLA – Test Generation - DFT Schemes — Built in Self Test.

UNIT IV **SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES** **9**

Programming Logic Device Families — Designing a Synchronous Sequential Circuit using PLA/PAL – Designing ROM with PLA – Realization of Finite State Machine using PLD – FPGA –Xilinx FPGA - Xilinx 4000.

UNIT V **SYSTEM DESIGN USING VERILOG** **9**

Hardware Modeling with Verilog HDL – Logic System, Data Types And Operators For Modelling In Verilog HDL - Behavioral Descriptions In Verilog HDL – HDL Based Synthesis – Synthesis Of Finite State Machines– Structural Modeling – Compilation And Simulation Of Verilog Code – Test Bench - Realization Of Combinational And Sequential Circuits Using Verilog – Registers – Counters — FIFOs–Sequential Machine —Adder — Multiplier- Divider — Design Of Simple Microprocessor, Introduction To System Verilog.

TOTAL: 45 PERIODS

SUGGESTED ACTIVITIES:

1.	Design asynchronous sequential circuits

2.	Design synchronous sequential circuits using PLA/PAL
3.	Simulation of digital circuits in FPGA.
4.	Design digital systems with System Verilog.
PRACTICAL EXERCISES:	**30 PERIODS**
1.	Design of Registers by Verilog HDL.
2.	Design of Counters by Verilog HDL.
3.	Design of Sequential Machines by Verilog HDL.
4.	Design of Serial Adders, Multiplier and Divider by Verilog HDL.
5.	Design of a simple Microprocessor by Verilog HDL
	TOTAL: 75 PERIODS
COURSE OUTCOMES:	
At the end of the course, the students will be able to:	
CO1:	Infer the basic concept of combinational circuit, synchronous sequential circuits and architecture of programmable devices.
CO2:	Illustrate the testing procedure for combinational circuit and PLA.
CO3:	Construct the synchronous and asynchronous sequential circuits.
CO4:	Develop synchronous circuits using programmable devices.
CO5:	Use programming tools for implementing digital circuits for industry standards.
REFERENCES:	
1.	Charles H.Roth., "Fundamentals of Logic Design" Seventh Edition, Cengage Learning, 2014
2.	M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice Hall, 1999
3.	M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR), 1999.
4.	Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001.
5.	Paragk.Lala "Fault Tolerant and Fault Testable Hardware Design" B S Publications,2002.
6.	Paragk.Lala "Digital System Design Using PLD" B S Publications, 2003.
7.	Palnitkar , Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	1	1	1	1
CO2	2	1	1	1	1	1
CO3	2	1	1	1	1	1
CO4	2	1	1	1	1	1
CO5	2	1	1	1	1	1
CO	2	1	1	1	1	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit I : Sequential Circuit Design	2	1either or	1(2)-CO1	1(2)-CO1	1either or (16) CO1	-

Unit II: Asynchronous Sequential Circuit Design	2	1either or	1(2)-CO2	1(2)-CO2	1either or (16) CO2	-
Unit III: Fault Diagnosis And Testability Algorithms	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16) CO3	-	-
Unit IV: Synchronous Design Using Programmable Devices	2	1either or	2(2)-CO4	-	1either or (16)-CO4	-
Unit V : System Design Using Verilog	2	1either or		1(2)-CO5	1(2)-CO5 1either or (16)-CO5	-
Total Title : AE22202-ADVANCED DIGITAL SYSTEM DESIGN	10	5either or	5(2)	4(2) 1 either or (16)	1(2) 4 either or (16)	-
Total Marks	20	80	10	24	66	-
Weightage	20%	80%	10%	24%	66%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22103	**ELECTRONIC SYSTEM DESIGN LABORATORY**	**L**	**T**	**P**	**C**
		0	**0**	**4**	**2**

OBJECTIVES:

- Design of instrumentation amplifier and voltage regulator
- Design of PCB layout
- Write a Verilog HDL coding of various combinational circuits
- Verify the design functionality for various memory modules
- Design of PLL circuits

LIST OF EXPERIMENTS

1.	Design of a 4-20 mA transmitter for a bridge type transducer. Design the Instrumentation amplifier with the bridge type transducer (Thermistor or any resistance variation transducers) and convert the amplified voltage from the instrumentation amplifier to 4 —20 mA current using op-amp. Plot the variation of the temperature Vs output current.
2.	Design of AC/DC voltage regulator using SCR Design a phase controlled voltage regulator using full wave rectifier and SCR, vary the conduction angle and plot the output voltage.
3.	PCB layout design using CAD Drawing the schematic of simple electronic circuit and design of PCB layout using CAD

4.	HDL based design entry and simulation of Parameterizable cores of Counters, Shift registers, State machines, 8-bit Parallel adders and 8 –Bit multipliers.
5.	HDL based design entry and simulation of Parameterizable cores on the simple Distributed Arithmetic system. Test vector generation and timing analysis.
6.	HDL based design entry and simulation of Parameterizable cores on memory design and 4 — bit ALU. Synthesis, P&R and post P&R simulation, Critical paths and static timing analysis results to be identified. FPGA real time programming and I/O interfacing.
7.	Interfacing with Memory modules in FPGA Boards. Verifying design functionality by probing internal signals.
8.	Realization of Discrete Fourier transform/Fast Fourier Transform algorithm in HDL and observing the spectrum in simulation.
9.	Invoke PLL module and demonstrate the use of the PLL for clock generation in FPGAs. Verify design functionality implemented in FPGA by capturing the signal in Oscilloscope
	TOTAL: 60 PERIODS
COURSE OUTCOMES:	
At the end of the course, the students will be able to:	
CO1:	Design an instrumentation amplifier and voltage regulator
CO2:	Design a PCB layout using CAD tool
CO3:	Write a Verilog code for various combinational and sequential circuits
CO4:	Develop a memory module with FPGA
CO5:	Design an PLL circuit

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	-	2	2	1
CO2	-	1	2	-	1	-
CO3	1	-	2	2	-	1
CO4	2	1	1	-	-	2
CO5	-	1	2	-	-	-
CO	1.6	1	1.8	2	1.5	2

AE22104	**TECHNICAL SEMINAR**	**L**	**T**	**P**	**C**
		0	**0**	**2**	**1**
LIST OF EXPERIMENTS					
1.	Selecting a subject, narrowing the subject into a topic				
2.	Stating an objective.				
3.	Collecting the relevant bibliography (at least 15 journal papers)				
4.	Preparing a working outline.				
5.	Studying the papers and understanding the author’s contributions and critically analysing each paper.				
6.	Preparing a working outline				
7.	Linking the papers and preparing a draft of the paper.				
8.	Preparing conclusions based on the reading of all the papers.				
9.	Writing the Final Paper and giving final Presentation				
	TOTAL: 30 PERIODS				

Please keep a file where the work carried out by you is maintained.Activities to be carried out

Activity	Instructions	Submission week	Evaluation
Selection of area of interest and Topic Stating an Objective	You are requested to select an area of interest, topic and state an objective	2nd week	**3 %** Based on clarity of thought, current relevance and clarity in writing
Collecting Information about your area & topic	1. List 1 Special Interest Groups or professional society 2. List 2 journals 3. List 2 conferences, symposia or workshops 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularlyin your area 7. Attach a call for papers (CFP) from your area.	3rd week	**3%** (the selected information must bearea specific and of international and national standard)
Collection of Journal papers inthe topic in the context of the objective – collect20 & then filter	• You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar • When picking papers to read - try to: • Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, • Favour papers from well-known journals and conferences, • Favour "first" or "foundational" papers in the field (as indicated in other people's survey paper), • Favour more recent papers, • Pick a recent survey of the field so you can quickly gain an overview, • Find relationships with respect to each other and to your topic area (classification scheme/categorization) • Mark in the hard copy of paperswhether complete work or section/sections of the paper are being considered	4th week	**6%** (the list of standardpapers and reason for selection)
Reading and notes for first 5papers	Reading Paper Process • For each paper form a Tableanswering the following questions:	5th week	**8%** (the table given should indicate your

	• What is the main topic of the article? • What was/were the main issue(s)the author said they want to discuss? • Why did the author claim it was important? • How does the work build on other's work, in the author's opinion?		understanding of thepaper and the evaluation is based on your conclusions about each paper)
	• What simplifying assumptions doesthe author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)		
Reading and notes for next5papers	Repeat Reading Paper Process	6th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based onyour conclusions about each paper)
Reading and notes for final 5papers	Repeat Reading Paper Process	7th week	**8%** (the table given should indicate your understanding of the paper and the evaluation is based onyour conclusions about each paper)
Draft outline 1and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	**8%** (this component willbe evaluated based on the linking and classification amongthe papers)

Abstract	Prepare a draft abstract and give a presentation	9th week	**6%** (Clarity, purpose and conclusion) **6%** Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	**5%** (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11thweek	**10%** (this component will be evaluated based on the linking and classification among the papers)
Your conclusions	Write your conclusions and future work	12th week	**5%** (conclusions – clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th week	**10%** (formatting, English, Clarity and linking) **4%** Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th & 15thweek	**10%** (based on presentation and Viva-voce)

RM22101	**RESEARCH METHODOLOGY**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**2**
UNIT I	**RESEARCH DESIGN**				**6**
Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.					
UNIT II	**DATA COLLECTION AND SOURCES**				**6**
Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods.Data - Preparing, Exploring, examining and displaying.					
UNIT III	**DATA ANALYSIS AND REPORTING**				**6**
Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation.					
UNIT IV	**INTELLECTUAL PROPERTY RIGHTS**				**6**

Intellectual Property — The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTOin IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.		
UNIT V	**PATENTS**	**6**
Patents — objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents.		
		TOTAL: 30 PERIODS

REFERENCES:

1.	Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education, 11e (2012).
2.	Kothari C R, Gaurav Garg, "Research Methodology- Methods and Techniques" New Age International Publishers, 2019.
3.	Catherine J. Holland, "Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets", Entrepreneur Press, 2007.
4.	David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tool & techniques", Wiley, 2007.
5.	The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.

Table of specification for End semester question paper

Unit No. and Title	Total 2 Marks Qns.	Total 16 Marks Qns.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse (An) Evaluate (Ev)
			No. of Qns. (marks) and CO			
Unit-I: Research Design	2	1 either or	2(2) – CO1	1 either or (16) – CO1	-	-
Unit-II: Data Collection And Sources	2	1 either or	2(2) - CO2		1 either or (16) — CO2	-
Unit-III: Data Analysis And Reporting	2	1 either or	1(2) — CO3	1(2) — CO3		1 either or (16) — CO3
Unit-IV: Intellectual Property Rights	2	1 either or	2(2) - CO4		1 either or (16) — CO4	-
Unit-V: Patents	2	1 either or	1(2) – CO5	1(2) — CO5 1 either or (16) — CO5	-	
Total Qns. RESEARCH METHODOLOGY	10	5 either or	8(2)	2(2) 2 either or (16)	2 either or (16)	-
Total Marks	20	80	16	36	32	16
Weightage	20%	80%	16%	36%	32%	16%

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

SEMESTER II

AE22204	POWER CONVERSION CIRCUITS FOR ELECTRONICS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To provide the students a deep insight in to the working of different switching devices withrespect to their characteristics
- To analyze different converters with their applications
- To study advanced converters and switching techniques implemented in recent technology Pre requisites: Introductory physics, Electric networks, Basic electronics devices

UNIT I	POWER ELECTRONIC DEVICES AND SEMICONDUCTOR SWITCHES	9

Introduction, Applications of power electronics, Power electronics devices: Characteristics of power devices – characteristics of SCR, Diac, Triac, GTO, PUJT, power transistors – power FETs – LASCR – two transistor model of SCR Protection of Thyristors against over voltage – over current,dv/dt and di/dt. Power Semiconductor Switches: Rectifier diodes, fast recovery diodes.

UNIT II	SCR PERFORMANCE AND APPLICATIONS	9

Turn on circuits for SCR – triggering with single pulse and train of pulses synchronizing with supply Thyristor turn off methods, natural and forced commutation, self-commutation series and parallel operations of SCRs. Rectifiers: Single phase and three phase controlled Rectifiers with inductive loads, RL load. Construction & Working of Opto- Isolators, Opto-TRIAC, Opto-SCR.

UNIT III	INVERTERS AND VOLTAGE CONTROLLERS	9

Voltage and current source inverters, resonant, Series inverter, PWM inverter. AC and DC choppers – DC to DC converters – Buck, boost and buck – boost. Single phase and three phase Cyclo-conveters, Power factor control and Matrix Converters. Industrial applications DC and AC Drives DC Motor Speed control Induction Motor Speed Control.

UNIT IV	TIMERS & DELAY ELEMENTS, HIGH FREQUENCY POWER HEATING,SENSOR AND ACTUATORS	9

RC Base Constant Timers, Timer Circuits using SCR, IC-555, Programmable Timer and their Industrial Applications, Induction Heating and Dielectric Heating System and Their Applications, Sensors, Transducers, and Transmitters for Measurement, Control & Monitoring : Thermoresistive Transducer, Photoconductive Transducers, Pressure Transducers, Flow Transducers, Level Sensors, Speed Sensing, Vibration Transducers, Variable-Frequency Drives, Stepper Motors and Servomotor Drives.

UNIT V	AUTOMATION AND CONTROL	9

Data Communications for Industrial Electronics, Telemetry, SCADA & Automation, AC & DC Drives, Voltage & Power Factor Control through Solid State Devices, Soft Switching, Industrial Robots.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Explain the characteristics, operation of power switching devices and identify their ratings and applications.
CO2:	Illustrate the construction and performance of SCR.
CO3:	Construct the converter based on SCR for various industrial applications.
CO4:	Develop the ability to know heating systems, timers, relevant sensors & actuator and their application in Industrial Setting.
CO5:	Analyze the data communication, Telemetry & SCADA system in Industrial Applications.

REFERENCES:	
1.	Thomas E. Kissell, Industrial Electronics: Applications for Programmable Controllers, Instrumentation and Process Control, and Electrical Machines and Motor Controls, 3rd edition, 2003, Prentice Hall.
2.	B. Paul, Industrial Electronic and Control, Prentice Hall of India Private Limited (2004).
3.	M.H. Rashid, "Power Electronics: Circuits, Devices & Applications", Pearson Education India; fourth edition, 2017.
4.	Ned Mohan, T.M. Undeland and W.P. Robbins, "Power Electronics: Converters, Applications and Design", Wiley India Ltd, 2008.
5.	M.S. Jamil Asghar, "Power Electronics" Prentice Hall of India Ltd., 2004
6.	V.R. Moorthy, "Power Electronics: Devices, Circuits and Industrial Applications" OxfordUniversity Press, 2007.
7.	G.K. Dubey, Power Semiconductor Controlled Drives, Prentice Hall inc. (1989).
8.	J.M.D. Murphy, F.G. Turnbull, Power Electronic Control of AC Motors, Pergamon (1990).

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	2	1	1	1
CO2	2	1	2	1	1	1
CO3	2	1	2	1	1	1
CO4	2	1	2	1	1	1
CO5	2	1	2	1	1	1
CO	2	1	2	1	1	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit I Power Electronic Devices and Semiconductor Switches	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit II SCR Performance and Applications	2	1either or	1(2)-CO2	1(2)-CO2	1either or (16)-CO2	-
Unit III Inverters and Voltage Controllers	2	1either or	1(2)-CO3	1(2)-CO3	1either or (16)-CO3	-
Unit IV Timers & Delay Elements, High Frequency Power Heating, Sensor and Actuators	2	1either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4	-	-

Unit V Automation and Control	2	1either or	1(2)-CO5	1(2)-CO5 1either or (16)-CO5	-	-
Total Title : AE22204 - POWER CONSERVATION CIRCUITS FOR ELECTRONICS	10	5either or	6(2)	4(2) 3 either or (16)	2 either or (16)	-
Total Marks	20	80	12	56	32	-
Weightage	20%	80%	12%	56%	32%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22201	**SEMICONDUCTOR DEVICES AND MODELING**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To acquire the fundamental knowledge and to expose to the field of semiconductor theoryand devices and their applications
- To gain adequate understanding of semiconductor device modeling aspects, designingdevices for electronic applications
- To acquire the fundamental knowledge of different semiconductor device modeling aspects

UNIT I	**MOS CAPACITORS**	**9**

Surface Potential: Accumulation, Depletion, and Inversion, Electrostatic Potential and Charge Distribution in Silicon, Capacitances in an MOS Structure, Polysilicon-Gate Work Function and Depletion Effects, MOS under Non equilibrium and Gated Diodes, Charge in Silicon Dioxide and at the Silicon–Oxide Interface, Effect of Interface Traps and Oxide Charge on Device Characteristics, High-Field Effects, Impact Ionization and Avalanche Breakdown, Band-to-Band Tunneling, Tunneling into and through Silicon Dioxide, Injection of Hot Carriers from Silicon into Silicon Dioxide, High-Field Effects in Gated Diodes, Dielectric Breakdown.

UNIT II	**MOSFET DEVICES**	**9**

Long-Channel MOSFETs, Drain-Current Model, MOSFET I–V Characteristics, Subthreshold Characteristics, Substrate Bias and Temperature Dependence of Threshold Voltage, MOSFET Channel Mobility, MOSFET Capacitances and Inversion-Layer Capacitance Effect, Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport Channel Length Modulation, Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields

UNIT III	**CMOS DEVICE DESIGN**	**9**

CMOS Scaling, Constant-Field Scaling, Generalized Scaling, Nonscaling Effects, Threshold Voltage, Threshold-Voltage Requirement, Channel Profile Design, Nonuniform Doping, Quantum Effect on Threshold Voltage, Discrete Dopant Effects on Threshold Voltage, MOSFET Channel Length, Various Definitions of Channel Length, Extraction of the Effective Channel Length, Physical Meaning of Effective Channel Length, Extraction of Channel Length by C–V Measurements.

UNIT IV	**BIPOLAR DEVICES**	**9**

Modifying the Simple Diode Theory for Describing Bipolar Transistors, Ideal Current–Voltage Characteristics, Ideal IC–VCE Characteristics, Characteristics of a Typical n–p–n Transistor, Effect of Emitter and Base Series Resistances, Effect of Base–Collector Voltage on Collector Current, Collector Current Falloff at High Currents, Non ideal Base Current at Low Currents, Bipolar Device Models for Circuit and Time-Dependent Analyses Basic dc Model, Basic ac Model, Small-Signal Equivalent-Circuit Model, Emitter Diffusion Capacitance, Charge-Control Analysis, Breakdown Voltages, Common-Base Current Gain in the Presence of Base–Collector Junction Avalanche, Saturation Currents in a Transistor.		
UNIT V	**MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS**	**9**
Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.		
		TOTAL: 45 PERIODS
SUGGESTED ACTIVITIES:		**30 PERIODS**
1. Simulate characteristics of a simple semiconductor devices using MATLAB, SPICE and ATLAS / SYNOPSYS		
2. Compact models for MOSFET and their implementation in SPICE-		
3. Level 1, 2 and 3, MOS model parameters in SPICE		
		TOTAL: 75 PERIODS
COURSE OUTCOMES:		
At the end of the course, the students will be able to:		
CO1:	Explain the properties of MOS capacitors.	
CO2:	Illustrate the CMOS design parameters and their impact on performance of the device.	
CO3:	Summarize the device level characteristics of BJT transistors.	
CO4:	Identify the suitable mathematical technique for device simulation.	
CO5:	Analyze the various characteristics of MOSFET devices.	
REFERENCES:		
1.	Yuan Taur and Tak H.Ning, "Fundamentals of Modern VLSI Devices", Cambridge University Press, 2016.	
2.	A.B. Bhattacharyya “Compact MOSFET Models for VLSI Design”, John Wiley & Sons Ltd, 2009.	
3.	Ansgar Jungel, “Transport Equations for Semiconductors”, Springer, 2009	
4.	Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd, 2004	
5.	Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag., 1984	
6.	Behzad Razavi, “Fundamentals of Microelectronics” Wiley Student Edition, 2nd Edition,2014	
7.	J P Collinge, C A Collinge, “Physics of Semiconductor devices” 2 nd Edition, Springer, 2006	
8.	S.M.Sze, Kwok.K. NG, “Physics of Semiconductor devices”, Springer, 2006	

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	2	1	1	1
CO2	2	1	2	1	1	1
CO3	2	1	2	1	2	2
CO4	2	1	2	1	1	1
CO5	2	1	2	1	2	2
CO	2	1	2	1	1.4	1.4

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit I : MOS CAPACITORS	2	1either or	2(2)- CO1	1either or (16)-CO1	-	-
Unit-II: MOSFET DEVICES	2	1either or	1(2)-CO2	1(2)-CO2 1either or (16)-CO2		-
Unit-III: CMOS DEVICE DESIGN	2	1either or	-	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-
Unit-IV: BIPOLAR DEVICES	2	1either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4	-	-
Unit-V: MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS	2	1either or	1(2)-CO5	1(2)-CO5 1either or (16)-CO5	-	-
Total Title : AE22201 - SEMICONDUCTOR DEVICES AND MODELING	10	5either or	5(2)	4(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	10	72	18	-
Weightage	20%	80%	10%	72%	18%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22202	**ADVANCED DIGITAL SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To describe fundamental concepts of DSP and Discrete Transforms
- To design digital filters design
- To estimate power spectrum using non- parametric and parametric methods
- To analyze the Multirate Signal processing by decimation and interpolation.
- To apply the concept of Multirate signal processing for various applications

UNIT I	**DIGITAL SIGNAL PROCESSING**	**9**

Sampling of analog signals - Selection of sampling frequency - Frequency response - Transfer functions - Filter structures - Fast Fourier Transform (FFT) Algorithms - Image coding - DCT.

UNIT II	**DIGITAL FILTER DESIGN**	**9**

IIR and FIR Filters: Filter structures, Implementation of Digital Filters - 2nd Order Narrow Band Filter and 1st Order All Pass Filter, Frequency sampling structures of FIR, Lattice structures, Forward and Backward prediction error filters, Reflection coefficients for lattice realization,

Implementation of lattice structures for IIR filters, Advantages of lattice structures.		
UNIT III	**ESTIMATION OF POWER SPECTRUM**	**9**
Non-Parametric Methods: Estimation of spectra from finite duration observation of signals,: Bartlett, Welch & Blackman-Tukey methods, Performance Comparison. Parametric Methods: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation.		
UNIT IV	**MULTI RATE SIGNAL PROCESSING**	**9**
Decimation by a factor D - Interpolation by a factor I - Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design and Implementation for sampling rate conversion. Up-sampling using All Pass Filter.		
UNIT V	**APPLICATIONS OF MULTI RATE SIGNAL PROCESSING AND DSP INTEGRATED CIRCUITS**	**9**
Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Subband Coding of Speech Signals, Quadrature Mirror Filters, Over Sampling A/D and D/A Conversion.		
		TOTAL: 45 PERIODS
SUGGESTED ACTIVITIES:		**30 PERIODS**
1. Design of Adaptive channel equalizer		
2. Realization of sub band filter using linear convolution		
3. Realization of STFT using FFT		
4. Demonstration of Bayes technique		
5. Demonstration of Min-max technique		
6. Realization of FIR Wiener filter		
7. Generation of Multivariate Gaussian generated data with desired mean vector and the required co-variance matrix		
8. Design and Realization of the adaptive filter using LMS algorithm (solved using steepest-descent algorithm)		
9. Representation of the 2D image signal as the linear combinations of PCA (Eigen faces)		
10. Image compression using Discrete cosine transformation (DCT).		
11. Multiple-input Multiple output (MIMO)		
12. Speech recognition using Support Vector Machine (SVM)		
		TOTAL: 75 PERIODS
COURSE OUTCOMES:		
At the end of the course, the students will be able to:		
CO1:	Explain the basics of Digital Signal Processing, Discrete Time Transforms and DSP Integrated circuits	
CO2:	Construct FIR/IIR digital filters using various structures	
CO3:	Discuss the various field effects in digital signal processing and the procedure involved in the fabrication of DSP Integrated circuits	
CO4:	Analyze the applications of multi rate signal processing at different sampling frequencies	
CO5:	Analyze multi rate signal processing and power spectrum using appropriate parametric/non-parametric methods	
REFERENCES:		
1.	J.G.Proakis & D. G.Manolakis Digital Signal Processing: Principles, Algorithms & Applications -, 4th Ed., Pearson Education, 2013	
2.	Frederic J Harris," Multirate Signal Processing for Communication Systems", 2nd Edition, River Publishers Series in Signal, Image and Speech Processing, USA, 2021.	
3.	Salivahanan," Digital Signal Processing",4th Edition,McGraw Hill,2019.	

4.	Shivkumar Venkatraman Iyer," Digital Filter Design using Python for Power Engineering Applications", Springer Nature,2020.
5.	Alan V Oppenheim & Ronald W Schaffer Discrete Time signal processing, Pearson Education, 2014.
6.	Keshab K. Parhi, 'VLSI Digital Signal Processing Systems Design and Implementation", John Wiley& Sons, 2007
7.	Steven. M .Kay, Modern Spectral Estimation: Theory & Application –PHI, 2009
8.	P.P.Vaidyanathan, Multi Rate Systems and Filter Banks , Pearson Education, 1993

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	2	2	2	1
CO2	2	1	2	2	2	1
CO3	2	1	2	2	2	1
CO4	2	1	2	2	2	1
CO5	2	1	2	2	2	1
CO	**2**	**1**	**2**	**2**	**2**	**1**

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: DIGITAL SIGNAL PROCESSING	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: DIGITAL FILTER DESIGN	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: ESTIMATION OF POWER SPECTRUM	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: MULTI RATE SIGNAL PROCESSING	2	1either or	1(2)-CO3	1(2)-CO3	1either or (16)-CO4	-
Unit-V: APPLICATIONS OF MULTI RATE SIGNAL PROCESSING AND DSP INTEGRATED CIRCUITS	2	1either or	1(2)-CO3	1(2)-CO5 1either or (16)-CO5		-
Total Qns. Title:	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-

Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22203	**EMBEDDED SYSTEMS**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- Learn Embedded design challenges and design methodologies
- Study general and single purpose processor
- Understand bus structures
- Design a state machine and concurrent process models
- Know about Embedded software development tools and RTOS

UNIT I	**EMBEDDED SYSTEM OVERVIEW**	**9**

Embedded System Overview, Design Challenges — Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

UNIT II	**GENERAL AND SINGLE PURPOSE PROCESSOR**	**9**

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer's view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III	**BUS STRUCTURES**	**9**

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, WirelessProtocols – IrDA, Bluetooth, IEEE 802.11.

UNIT IV	**STATE MACHINE AND CONCURRENT PROCESS MODELS**	**9**

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models

UNIT V	**EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS**	**9**

Compilation Process — Libraries — Porting kernels — C extensions for embedded systems — emulation and debugging techniques – RTOS – System design using RTOS. Case study: Embedded system in IOT.

TOTAL:45 PERIODS

SUGGESTED ACTIVITIES:

1: Insist students to write a requirements form for a smart phone

2: Compare different Microcontrollers for a particular ESD.

3: Application of a protocol for a specified application.

4: Write an Embedded C code for a given task.

5: Design an Embedded system for any type of real time application

PRACTICAL LIST: **30 PERIODS**

Exercise – 1

Comparative study of software development tools and design steps with respect to FPGA

based and Non – FPGA based (defined logic) embedded system development. (For Example: consider any Spartan FPGA board for FPGA based Embedded System Considerany cortex-M based board for Non – FPGA based Embedded system)

Exercise – 2

Implement adder and decoder logic blocks in any one of the FPGA chip based development board.

Exercise – 3

Design and development of UART protocol logic block in any one of FPGA chip based development board.

Exercise – 4

Consider on board LEDS (any four) and timer logic block of cortex- M board. Write a program which enables LEDS to glow in different timing

Exercise – 5

Consider on board switches and (2x16) LCD display develop a program which displays the status of switch activation

Exercise – 6

Demonstrate GPIO based I/O interfacing by considering LM 35 temperature sensor and cortex-M board

Exercise – 7

Development of one interfacing scheme which transmits data from one cortex- M board to another cortex- M board using on chip CAN logic blocks

Exercise – 8

Consider on board EPROM IC of Cortex- M board by utilizing on chip I2c logic block transmit data to EPROM IC and receive stored data from EPROM IC

Exercise – 10

Consider two ultrasonic sensors which are interfaced with cortex- M board. Both are located some distance (2 meters) apart vertically so that the system can identify the movement of object in term of distance. consider data reception and display of each sensor as two different tasks by RTOS. Establish a RTOS based system to recognize the height of moving object

OBJECTIVE:

- Able to understand embedded system design flow in FPGA chip based and Non – FPGA chip based embedded development boards
- Able to create simple logic blocks in FPGA chip based boards
- Able to understand interfacing scheme for Non – FPGA board scheme for Non – FPGA
- Able to utilize RTOS functions for interfacing practice

REQUIREMENTS:

Hardware and Software requirements

1. Cortex- M board and simulation tools
2. FPGA EVM Board and simulation tools
3. Ultrasonic sensor
4. Any portable open source RTOS

TOTAL : 75 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Explain Embedded System architecture, different protocols and its overview.
CO2:	Summarize the general and single purpose processor.
CO3:	Interpret the different bus protocols
CO4:	Illustrate state machine and design process models
CO5:	Outline embedded software development tools and RTOS

CO6:	Develop simple logic blocks in FPGA chip-based boards.

REFERENCES:

1.	Marilyn Wolf, "Embedded System Interfacing: Design for the Internet-of-Things (IoT) and Cyber-Physical Systems(CPS)", Elsevier, 4th Edition 2019.
2.	Cem Unsalan, Huseyin Deniz Gurhan, Mehmet Erkin Yucel, "Embedded System Design with Arm Cortex-M Microcontrollers: Applications with C, C++ and MicroPython", Springer, 2022.
3.	Frank Vahid and Tony Gwargie, "Embedded System Design", John Wiley & sons, 2002.
4.	Steve Heath, "Embedded System Design", Elsevier, Second Edition, 2004
5.	Arockia Bazil Raj A., " Embedded System Developer's Guide", CRC Press, 2018.
6.	Jim Ledin, "Architecting High-Performance Embedded Systems: Design and build high-performance real-time digital systems based on FPGAs and custom circuits", Packt Publishing, 2021.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	-	2	1	2	1
CO2	2	-	2	1	2	1
CO3	2	-	2	1	2	1
CO4	2	-	2	1	2	1
CO5	2	-	2	1	2	1
CO	2	-	2	1	2	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: EMBEDDED SYSTEM OVERVIEW	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: GENERAL AND SINGLE PURPOSE PROCESSOR	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: BUS STRUCTURES	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: STATE MACHINE AND CONCURRENT PROCESS MODELS	2	1either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4	-	-
Unit-V: EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS	2	1either or	2(2)-CO5	1either or (16)-CO5		-

Total Qns. Title: AE22203 : EMBEDDED SYSTEMS	10	5either or	8(2)	2(2) 5 either or (16)	-	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22205	**VLSI DESIGN LABORATORY**	**L**	**T**	**P**	**C**
		0	**0**	**4**	**2**

OBJECTIVES:

- Familiarize with different FPGA boards
- Analyze digital design using Front end Tools
- Analyze the CMOS circuits using CAD tools
- Analyze the interfacing of I/O devices with Arduino Boards using Embedded C

LIST OF EXPERIMENTS

1.	Synthesize and implement Combinational and Sequential Circuits in VERILOG /VHDL
2.	Synthesize and implement MAC unit and GCD unit in Verilog /VHDL
3.	Implementation of sampling of input signal and display in FPGA Synthesize and implement FIR filter and IIR filter Verilog /VHDL
4.	Synthesize and implement 8 bit general purpose processor in Verilog/VHDL
5.	Synthesize and implement UART and USART
6.	Simulation and Analysis of CMOS combinational and sequential logic circuits using CAD tools

TOTAL: 60 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Program in Verilog/VHDL for combinational and sequential circuits and implement the program in FPGA
CO2:	Implement FIR and IIR filters in FPGA
CO3:	Implement data path design and interfaces
CO4:	Handle CAD tools to draw/edit, and analyze the CMOS circuits.
CO5:	Program and interface the Arduino Boards using Embedded C

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	**Programme Outcomes**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	-	2	2	1
CO2	-	1	2	-	1	-
CO3	1	-	2	2	-	1
CO4	2	1	1	-	-	2
CO5	-	1	2	-	-	-
CO	1.6	1	1.8	2	1.5	1.3

RM22201	RESEARCH TOOLS LABORATORY	L	T	P	C
		0	0	4	2

OBJECTIVES:

- To familiarize the fundamental concepts/techniques for Project Management
- To familiarize the journal paper formatting using suitable Software
- To familiarize the software for literature review and Bibliography
- To find the plagiarism percentage of article contents
- To prepare a quality research report and the presentation

LIST OF EXPERIMENTS

1.	Use of tools / Techniques for Research - Project management -Microsoft Project / Microsoft OneNote / Asana.
2.	Hands on Training related to Software for Paper Formatting like LaTeX / MS Office
3.	Design a Layout of a Research Paper - Guidelines for Submitting the Research Paper - Review Process -Addressing Reviewer Comments.
4.	Introduction to Data Analysis Software - Origin SPSS, ANOVA etc.,
5.	Introduction to Software for detection of Plagiarism – Urkund, Turniton
6.	Preparing Bibliography / Different Reference Formats. – EndNote, Mently
7.	Format of Project Report - Use of Quotations - Method of Transcription- Elements: Title Page - Abstract - Table of Contents - Headings and Sub-Headings - Footnotes - Tables and Figures
8.	Introduction to Microsoft Excel –for Research Analysis
9.	Presentation using PPTs.

TOTAL: 60 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	List the various stages in research and develop systematic planning of project stages. (Analysing)
CO2:	Write a journal paper and formulate as per the standard journal format (Applying)
CO3:	Develop a literature review and relevant references for a research problem using suitable(Applying)
CO4:	Determine the plagiarism of the article / report content by using the Software (Applying)
CO5:	Compile a research report and the presentation (Applying)

SEMESTER III

AE22301	INPLANT / INDUSTRIAL / PRACTICAL TRAINING	L	T	P	C
		0	0	4	2

COURSE OBJECTIVE:

- To train the students in the field work so as to have first-hand knowledge of practical problems in carrying out engineering tasks.

SYLLABUS:

The students individually undertake training in reputed companies /organization during the summer vacation for a specified duration of four weeks. At the end of training, a detailed report on the work done should be submitted within ten days from the commencement of the semester. The students will be evaluated through a viva-voce examination by a team of internal staff.

TOTAL: 120 PERIODS

AE22302	PROJECT WORK I	L	T	P	C
		0	0	6	3

COURSE OBJECTIVES:

- To identify a specific problem for the current need of the society and collecting information related to the same through detailed review of literature.
- To develop the methodology to solve the identified problem.
- To train the students in preparing project reports and to face reviews and viva-voce examination.

SYLLABUS:

The student individually works on a specific topic approved by faculty member who is familiar in this area of interest. The student can select any topic which is relevant to his/her specialization of the programme. The topic may be experimental or analytical or case studies. At the end of the semester, a detailed report on the work done should be submitted which contains clear definition of the identified problem, detailed literature review related to the area of work and methodology for carrying out the work. The students will be evaluated through a viva-voce examination by a panel of examiners including one external examiner.

TOTAL: 90 PERIODS

COURSE OUTCOME:

At the end of the course, the students will be able to:

CO1:	Develop the ability to solve a specific problem right from its identification and literature review till the successful solution and prepare project reports.

SEMESTER IV

AE22401	PROJECT WORK II	L	T	P	C
		0	0	24	12

COURSE OBJECTIVES:

- To solve the identified problem based on the formulated methodology.
- To develop skills to analyze and discuss the test results, and make conclusions

SYLLABUS

The student should continue the phase I work on the selected topic as per the formulated methodology / Undergo internship. At the end of the semester, after completing the work to the satisfaction of the supervisor and review committee, a detailed report should be prepared and submitted to the head of the department. The students will be evaluated based on the report and the viva-voce examination by a panel of examiners including one external examiner.

TOTAL : 360 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1	Discover potential research areas
CO2	Apply the knowledge gained from theoretical and practical courses to be creative, well-planned, organized and coordinated
CO3	Represent data acquired in graphical and reader-friendly formats
CO4	Derive detailed conclusions from work carried out
CO5	Report and present the findings of the work conducted

PROFESSIONAL ELECTIVES

SEMESTER I, PROFESSIONAL ELECTIVE I

AE22111	APPLICATIONS SPECIFIC INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To analyze the issues and tools related to ASIC/FPGA design and implementation.
- To understand basics of System on Chip and Platform based design.

UNIT I	INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN	9

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell -Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II	PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS	9

Anti-fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX -Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III	PROGRAMMABLE ASIC ARCHITECTURE	9

Architecture and configuration of Spartan / Cyclone and Virtex / Stratix FPGAs — Micro-Blaze /Nios based embedded systems – Signal probing techniques.

UNIT IV	LOGIC SYNTHESIS, SYSTEM PARTITIONING, PLACEMENT AND ROUTING	9

Logic synthesis - System partitioning- ASIC floor planning- placement and routing – power and clocking strategies.

UNIT V	HIGH PERFORMANCE ALGORITHMS FOR ASICs/ SOCs. SOC CASE STUDIES	9

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators.Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Recall the CMOS logics, ASIC library and programmable ASICs
CO2:	Explain ASIC design flow, programmable ASIC cells and architectures
CO3:	Describe I/O cells, interconnects Tentative and high performance algorithms for ASICs
CO4:	Demonstrate logic synthesis, system partitioning, placement and routing
CO5:	Investigate new developments in SOC and low power design

REFERENCES:

1.	Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1997.
2.	Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunicationand Signal Processing", Prentice Hall, 1994.
3.	M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2014.
4.	Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994.
5.	Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation of Signal Processing Systems”, Wiley, 2008.
6.	Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science,2007

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	-	2	2	1	1
CO2	2	-	2	2	1	1
CO3	2	-	2	2	1	1
CO4	2	-	2	2	1	1
CO5	2	-	2	2	1	1
CO	2	-	2	2	1	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: Introduction To ASICs, CMOS Logic and ASIC Library Design	2	1 either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: Programmable ASICs, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells	2	1 either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: Programmable ASIC Architecture	2	1 either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: Logic Synthesis, System Partitioning, Placement and Routing	2	1 either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4	-	-
Unit-V: High Performance Algorithms For ASICs/SOCs. SOC Case Studies	2	1 either or	1(2)-CO5	1(2)-CO5 1either or (16)-CO5	-	-
Total Qns.	10	5 either or	7(2)	3(2) 5 either or (16)	-	-
Total Marks	20	80	14	86	-	-
Weightage	20%	80%	14%	86%	-	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22112	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To gain broad conceptual understanding of the various aspects of electromagnetic (EM)interference and compatibility
- To develop a theoretical understanding of electromagnetic shielding effectiveness
- To understand ways of mitigating EMI by using shielding, grounding and filtering
- To understand the need for standards and to appreciate measurement methods
- To understand how EMI impacts wireless and broadband technologies

UNIT I	INTRODUCTION & SOURCES OF EM INTERFERENCE	9

Introduction - Classification of sources - Natural sources - Man-made sources - Survey of the electromagnetic environment.

UNIT II	EM SHIELDING	9

Introduction -– Shielding Theory- LF Magnetic shielding, PCB level Shielding- Shielding effectiveness - Far-field sources - Near-field sources - Low-frequency,magnetic field shielding - Effects of apertures.

UNIT III	INTERFERENCE CONTROL TECHNIQUES	9

Equipment screening - Cable screening - grounding - Power-line filters - Isolation - Balancing - Signal-line filters - Nonlinear protective devices.

UNIT IV	EMC STANDARDS, MEASUREMENTS AND TESTING	9

Need for standards - Civilian EMC standards – Military standards - The international framework - Human exposure limits to EM fields -EMC measurement techniques - Measurement tools - Test environments. Need for standards - The international framework - Human exposure limits to EM fields –EMC measurement techniques - Measurement tools - Test environments.

UNIT V	EMC CONSIDERATIONS IN WIRELESS AND BROAD BAND TECHNOLOGIES	9

Efficient use of frequency spectrum - EMC, interoperability and coexistence - Specifications and alliances - Transmission of high-frequency signals over telephone and power networks — EMC and digital subscriber lines - EMC and power line telecommunications.

TOTAL: 45 PERIODS

SUGGESTED ACTIVITIES:

- Investigate various case studies related to EMIC. Example: Chernobyl Disaster in 1986.
- Develop some understanding about the design of EM shields in electronic system design and packaging.

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Demonstrate knowledge of the various sources of electromagnetic interference
CO2:	Display an understanding of the effect of how electromagnetic fields couple through apertures, and solve simple problems based on that understanding
CO3:	Explain the EMI mitigation techniques of shielding and grounding
CO4:	Explain the need for standards and EMC measurement methods
CO5:	Discuss the impact of EMC on wireless and broadband technologies

REFERENCES:

1.	Christopoulos C, Principles and Techniques of Electromagnetic Compatibility, CRC Press,Second Edition, Indian Edition, 2013.
2.	Paul C R, Introduction to Electromagnetic Compatibility, Wiley India, Second Edition, 2008.
3.	Kodali V P, Engineering Electromagnetic Compatibility, Wiley India, Second Edition,

	2010.
4.	Henry W Ott, Electromagnetic Compatibility Engineering, John Wiley & Sons Inc, Newyork, 2009.
5.	Scott Bennett W, Control and Measurement of Unintentional Electromagnetic Radiation, John Wiley& Sons Inc., Wiley Interscience Series, 1997.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	2	2	1	1	2
CO2	2	2	2	1	1	2
CO3	2	2	2	1	1	2
CO4	2	2	2	1	1	2
CO5	2	2	2	1	1	2
CO	**2**	**2**	**2**	**1**	**1**	**2**

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qns.	Total 16 Marks Qns.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: Introduction & Sources of EM Interference	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: EM Shielding	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: Interference Control Techniques	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: EMC Standards, Measurements and Testing	2	1either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4	-	-
Unit-V: EMC Considerations in Wireless and Broadband Technologies	2	1either or	1(2)-CO5	1(2)-CO5 1either or (16)-CO5	-	-
Total Qns.	10	5either or	7(2)	3(2) 5 either or (16)	-	-
Total Marks	20	80	14	86	-	-
Weightage	20%	80%	14%	54%	-	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22113	ANALOG AND MIXED SIGNAL IC DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To study the concepts of MOS large signal model and small signal model
- To provide in-depth understanding of the analog integrated circuit and building blocks
- To learn the Analog and Digital layout design for mixed signal circuits
- To understand the methodologies for analysis and design of fundamental CMOS Analog andMixed signal Circuits like Data Converters and filters.
- To study the integrated circuits like oscillators and PLLs.

UNIT I	INTRODUCTION AND BASIC MOS DEVICES	9

Challenges in analog design-Mixed signal layout issues- MOS FET structures and characteristics- large signal model – small signal model- single stage Amplifier-Source follower-Common gate stage – Cascade Stage

UNIT II	SUB-MICRON CIRCUIT DESIGN	9

Submicron CMOS process flow, Capacitors and resistors, Current mirrors, The MOSFET Switch, Analog Circuit Design: Biasing, Op-Amp Design, Circuit Noise - OP Amp parameters

UNIT III	DATA CONVERTERS	9

Characteristics of Sample and Hold- Digital to Analog Converters- architecture-Differential Non linearity-Integral Non linearity- Voltage Scaling-Cyclic DAC-Pipeline DAC-Analog to Digital Converters- architecture – Flash ADC-Pipeline ADC-Differential Non linearity-Integral Non linearity. Overview of SNR of Data Converters- Clock Jitters- Improving using Averaging – Decimating Filters for ADC- Band pass and High Pass Sinc Filters- Interpolating Filters for DAC

UNIT IV	ANALOG AND DIGITAL LAYOUT DESIGN FOR MIXED SIGNAL	9

Layout introduction: Introduction, , symbolic diagram. Digital layout design: Introduction, guide line of transistor layout, PMOS and NMOS transistor layout, CMOS transistor layout. Introduction to analog layout techniques and Passive component layout - capacitor, resistor and inductor, Floor planning of analog and digital components, power supply and ground pin issues, matching, shielding, interconnection issues

UNIT V	OSCILLATORS AND PLL	9

Voltage Controlled Oscillators. Simple PLL, Charge pumps PLLs, Non ideal effects in PLLs, Delay Locked Loops frequency multiplication and synthesis. Introduction to RF IC Design, building blocks, applications

TOTAL: 45 PERIODS

SUGGESTED ACTIVITIES:

- ICT/MOOCs Reference : https://nptel.ac.in/courses/117/101/117101105/

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Demonstrate the development in the area of analog and mixed signal IC design
CO2:	Enumerate the MOS fundamentals, small signal models and analysis of MOSFET based circuits
CO3:	Model data converter architectures
CO4:	Survey different mixed signal circuits for various applications as per the user specifications
CO5:	Examine and design mixed signal circuits such as Comparator, ADCs, DACs, PLL

REFERENCES:

1.	P. Allen and D. Holberg, “CMOS Analog Circuit Design”, Oxford University Press, Second Edition, 2012.
2.	B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, Second Edition 2017.

3.	R.Jacob Baker,H.W.Li, and D.E. Boyce CMOS Circuit Design ,Layout and Simulation, Prentice-Hall of India, Third Edition 2010.
4.	Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley Publishers, Fifth Edition, 2009.
5.	Behzad Razavi" Design of CMOS Phase –Locked Loops: from circuit level to architecture level" Cambridge University Press, 2020

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Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	2	2	2	2
CO2	2	1	2	2	2	2
CO3	2	1	2	2	2	2
CO4	2	1	2	2	2	2
CO5	2	1	2	2	2	2
CO	2	1	2	2	2	2

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit I Introduction and Basic MOS Devices	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit II Submicron Circuit Design	2	1either or	1(2)-CO2	1(2)-CO2	1either or (16)-CO2	-
Unit III Data Converters	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3		-
Unit IV Analog and Digital Layout Design or Mixed Signal	2	1either or	1(2)-CO4	1(2)-CO4	1either or (16)-CO4	-
Unit V Oscillators and PLL	2	1either or	1(2)-CO5	1(2)-CO5 1either or (16)-CO5	-	-
Total Title: Analog And Mixed Signal IC Design	10	5either or	6(2)	4(2) 3 either or (16)	2 either or (16)	-
Total Marks	20	80	12	56	32	-
Weightage	20%	80%	12%	56%	32%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20

Weightage	20%	20%	20%	20%	20%

AE22114	**VLSI TESTING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To introduce the VLSI testing
- To introduce logic and fault simulation and testability measures
- To study the test generation for combinational and sequential circuits
- To study the design for testability
- To study the fault diagnosis

UNIT I	**INTRODUCTION TO TESTING**	**9**

Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing - TestEconomics and Product Quality – Fault Modeling – Relationship Among Fault Models.

UNIT II	**LOGIC & FAULT SIMULATION & TESTABILITY MEASURES**	**9**

Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation –Algorithms for True Value and Fault Simulation – Scoap Controllability and Observability

UNIT III	**TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS**	**9**

Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG

UNIT IV	**DESIGN FOR TESTABILITY**	**9**

Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture – Built-in Self-Test – Random Logic Bist – DFT for Other Test Objectives, Memory Testing

UNIT V	**FAULT DIAGNOSIS**	**9**

Introduction and Basic Definitions – Fault Models for Diagnosis – Generation of Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Explain the basics of VLSI Testing Process and fault diagnosis
CO2:	Describe the concept of design for testability and fault simulation
CO3:	Perform analysis on design for testability and Fault Diagnosis
CO4:	Examine the Test generation for Combinational and Sequential Circuits
CO5:	Analyze Logic and Fault Simulation

REFERENCES:

1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, “VLSI Test Principles and Architectures”, Elsevier, 2017
2. Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2017.
3. Niraj K. Jha and Sandeep Gupta, “Testing of Digital Systems”, Cambridge University Press, 2017.
4. N. Jha& S.D. Gupta, “Testing of Digital Systems”, Cambridge, 2003.
5. W. W. Wen, “VLSI Test Principles and Architectures Design for Testability”, Morgan Kaufmann Publishers. 2006.
6. P. K. Lala,” Digital circuit Testing and Testability”, Academic Press. 1997.
7. M. Abramovici, M. A. Breuer, & A.D. Friedman, “Digital System Testing and Testable Design”, Computer Science Press, 1990.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	-	1	2	1	-
CO2	1	-	1	2	-	-
CO3	1	-	1	2	1	-
CO4	1	-	1	2	-	-
CO5	1	-	1	2	1	-
CO	1	-	1	2	**1**	-

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: INTRODUCTION TO TESTING	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: LOGIC & FAULT SIMULATION & TESTABILITY MEASURES	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III:TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV:. DESIGN FOR TESTABILITY	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO4		-
Unit-V:FAULT DIAGNOSIS	2	1either or	1(2)-CO3	1(2)-CO5	1either or (16)-CO5	-
Total Qns. Title: AE22114 VLSI TESTING	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22115	**SOFT COMPUTING AND OPTIMIZATION TECHNIQUES**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**
COURSE OBJECTIVES:					
• To classify various soft computing frame works					
• To be familiar with the design of neural networks, fuzzy logic, and fuzzy systems					

• To learn mathematical background for optimized genetic programming		
• Be exposed to neuro-fuzzy hybrid systems and its applications		
• To understand the various evolutionary optimization techniques		
UNIT I	**FUZZY LOGIC**	**9**
Introduction to Fuzzy logic - Fuzzy sets and membership functions- Operations on Fuzzy sets- Fuzzy relations, rules, propositions, implications, and inferences- Defuzzification techniques- Fuzzy logic controller design- Some applications of Fuzzy logic		
UNIT II	**ARTIFICIAL NEURAL NETWORKS**	**9**
Supervised Learning: Introduction and how brain works, Neuron as a simple computing element, The perceptron, Back propagation networks: architecture, multilayer perceptron, back propagation learning-input layer, accelerated learning in multilayer perceptron, The Hopfield network, Bidirectional associative memories (BAM), RBF Neural Network. Unsupervised Learning: Hebbian Learning, Generalized Hebbian learning algorithm, Competitive learning, Self-Organizing Computational Maps: Kohonen Network		
UNIT III	**GENETIC ALGORITHM**	**9**
Genetic algorithm- Introduction - biological background - Genetic basic concepts - operators – Encoding scheme – Fitness evaluation – crossover - mutation - Travelling Salesman Problem, Particle swam optimization, Ant colony optimization		
UNIT IV	**NEURO-FUZZY MODELING**	**9**
Adaptive Neuro-Fuzzy Inference Systems (ANFIS) – architecture - Coactive Neuro-Fuzzy Modeling, framework, neuron functions for adaptive networks – Data Clustering Algorithms – Rulebase Structure Identification –Neuro-Fuzzy Control – the inverted pendulum system		
UNIT V	**CONVENTIONAL OPTIMIZATION TECHNIQUES**	**9**
Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method		
TOTAL:45 PERIODS		
COURSE OUTCOMES:		
At the end of the course, the students will be able to:		
CO1:	Summarize the application on different soft computing techniques like Fuzzy, GA and Neural network	
CO2:	Explain Neuro-Fuzzy and Neuro-Fuzzy-GA expert system.	
CO3:	Solve machine learning problems through Neural networks.	
CO4:	Examine Neuro- Fuzzy system for clustering and classification.	
CO5:	Design optimization techniques to solve the real world problems.	
REFERENCES:		
1.	J.S.R.Jang, C.T. Sun and E.Mizutani, Neuro-Fuzzy and Soft Computing, PHI / Pearson Education 2004.	
2.	Timothy J. Ross," Fuzzy Sets and Fuzzy Logic with Engineering Applications",4th Edition, An Indian Adaptation,2021.	
3.	Jang , Sun and Mizutani," Neuro-Fuzzy And Soft Computing: A Computational Approach To Learning And Machine Intelligence", 1st Edition, Pearson India,2015.	
4.	Daniel Graupe," Principles Of Artificial Neural Networks: Basic Designs to Deep Learning",4th Edition, World Scientific, 2020.	
5.	David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addisonwesley, 2009.	
6.	Himanshu Singh&Yunis Ahmed Lone," Deep Neuro-Fuzzy Systems With Python", Apress publishers, 2020.	
7.	Sivanandam," Introduction To Genetic Algorithms", Springer India, 2013.	

8.	George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,PrenticeHall, 1995.
9.	James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, andProgramming Techniques, Pearson Edn., 2003.
10.	Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing,Prentice-Hall of India, 2003.
11.	Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 1998.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	2	2	2	2
CO2	2	1	2	2	2	2
CO3	2	1	2	2	2	2
CO4	2	1	2	2	2	2
CO5	2	1	2	2	2	2
CO	**2**	**1**	**2**	**2**	**2**	**2**

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: Fuzzy Logic	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: Artificial Neural Networks	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: Genetic Algorithm	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: Neuro-Fuzzy Modeling	2	1either or	1(2)-CO3	1(2)-CO3	1either or (16)-CO4	-
Unit-V: Conventional Optimization Techniques	2	1either or	1(2)-CO3	1(2)-CO5 1either or (16)-CO5		-
Total Qns. Title:	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

SEMESTER II, PROFESSIONAL ELECTIVE II

CU22322	RF SYSTEM DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- Be familiar with RF transceiver system design for wireless communications.
- Be exposed to design methods of receivers and transmitters used in communication systems
- Design RF circuits and systems using an advanced design tool .
- Exemplify different synchronization methods circuits and describe their block schematic and design criteria.
- Measure RF circuits and systems with a spectrum analyzer..

UNIT I	BASICS OF RADIO FREQUENCY SYSTEM DESIGN	9

Definitions and models of Linear systems and Non-linear system. Specification parameters: Gain, noise figure, SNR, Characteristic impedance, S-parameters, Impedance matching and Decibels. Elements of digital base band signaling: complex envelope of band pass signals, Average value, RMS value, Crest factor, Sampling, jitter, modulation techniques, filters, pulse shaping, EVM, BER, sensitivity, selectivity, dynamic range and, adjacent and alternate channel power leakages .

UNIT II	RADIO ARCHITECTURES AND DESIGN CONSIDERATIONS	9

Super heterodyne architecture, direct conversion architecture, Low IF architecture, band-pass sampling radio architecture, System Design Considerations for an Analog Frontend Receiver in Cognitive Radio Applications, Interference, Near, In-band & wide-band considerations

UNIT III	AMPLIFIER MODELING AND ANALYSIS	9

Noise: Noise equivalent model for Radio frequency device, amplifier noise model, cascade performance, minimum detectable signal, performance of noisy systems in cascade. Amplifier power relations, stability considerations, constant gain circles, constant VSWR circles, low noise circles broadband, high power and multistage amplifiers. Non-Linearity: Amplifier power transfer curve, gain compression, AM-AM, AM-PM, polynomial approximations, Saleh model, Wiener model and Hammerstein model, intermodulation, Single and two tone analyses, second and third order distortions and measurements, SOI and TOI points

UNIT IV	MIXER AND OSCILLATOR MODELING AND ANALYSIS	9

Mixers: Frequency translation mechanisms, frequency inversion, image frequencies, spurious calculations, principles of mixer realizations. Oscillators: phase noise and its effects, effects of oscillator spurious components, frequency accuracy, oscillator realizations: Frequency synthesizers, NCO.

UNIT V	APPLICATIONS OF SYSTEMS DESIGN	9

Multimode and multiband Super heterodyne transceiver: selection of frequency plan, receiver system and transmitter system design – Direct conversion transceiver: receiver system and transmitter system design

TOTAL:45 PERIODS

COURSE OUTCOMES:

Upon the completion of course, students will be able to

CO1:	Explain the specifications of transceiver modules and the principles of mixer and oscillator.
CO2:	Develop transceiver architectures and amplifier modelling.
CO3:	Apply the impact of noise in amplification modules and the resultant effect during cascade connections
CO4:	Examine spurs and generation principles during signal generation and frequency translations
CO5:	Design the transceivers for various RF applications.

REFERENCES:	
1.	Thomas H. Lee "The Design of CMOS Radio-Frequency Integrated Circuits" . Cambridge University Press, 2004.
2.	Qizheng Gu, "RF System Design of Transceivers for Wireless Communications", Springer ,2005
3.	Kevin McClaning, "Wireless Receiver Design for Digital Communications,". 2/3, Yes Dee Publications, 2012. .
4.	M C Jeruchim, P Balapan and K S Shanmugam, "Simulation of Communication systems:Modeling, Methodology and Techniques", Kluwer Academic/Plenum Publishers, 2nd Edition, 2000.
5.	Mike Golio and Janet Golio, "RF and Microwave Circuits, Measurements and Modeling", CRC Press, 2018.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	2	1	2	1	2
CO2	2	2	2	2	1	2
CO3	2	2	1	2	2	2
CO4	2	2	2	2	2	1
CO5	2	2	1	1	2	2
CO	2	2	1.4	1.8	1.6	1.8

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: BASICS OF RADIO FREQUENCY SYSTEM DESIGN	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: RADIO ARCHITECTURES AND DESIGN CONSIDERATIONS	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: AMPLIFIER MODELING AND ANALYSIS.	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: MIXER AND OSCILLATOR MODELING AND ANALYSIS.	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO4	-	-
Unit-V: APPLICATIONS OF SYSTEMS DESIGN.	2	1either or	1(2)-CO3	1(2)-CO5	1either or (16)-CO5	-
Total Qns. Title:	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-

Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22211	**ROBOTICS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To Introduce the concepts of Robotic systems
- To understand the concepts of Instrumentation and control related to Robotics
- To understand the kinematics and dynamics of robotics
- To explore robotics in Industrial applications

UNIT I	**INTRODUCTION TO ROBOTICS**	**9**

Robotics -History - Classification and Structure of Robotic Systems - Basic components -Degrees of freedom - Robot joints coordinates- Reference frames - workspace- Robot languages- Robotic sensors- proximity and range sensors, ultrasonic sensor, touch and slip sensor.

UNIT II	**ROBOT KINEMATICS AND DYNAMICS**	**9**

Kinematic Modelling: Translation and Rotation Representation, Coordinate transformation, DH parameters, Forward and inverse kinematics, Jacobian, Dynamic Modelling: Forward and inverse dynamics, Equations of motion using Euler-Lagrange formulation, Newton Euler formulation.

UNIT III	**ROBOTICS CONTROL**	**9**

Control of robot manipulator - state equations - constant solutions -linear feedback systems, single-axis PID control - PD gravity control -computed torque control, variable structure control and impedance control.

UNIT IV	**ROBOT INTELLIGENCE AND TASK PLANNING**	**9**

Artificial Intelligence - techniques - search problem reduction - predicate logic means and end analysis -problem solving -robot learning - task planning - basic problems in task planning - AI in robotics and Knowledge Based Expert System in robotics

UNIT V	**INDUSTRIAL ROBOTICS**	**9**

Robot cell design and control - cell layouts - multiple robots and machine interference - work cell design - work cell control - interlocks – error detection deduction and recovery - work cell controller - robot cycle time analysis. Safety in robotics, Applications of robot and future scope

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course the student will be able to

CO1:	Explain the fundamentals of robotics
CO2:	Illustrate the concept of kinematics and dynamics in robotics
CO3:	Analyze the robot control techniques
CO4:	Examine the basis of intelligence in robotics and task planning
CO5:	Discuss the industrial applications of robotics

REFERENCES:

1	John J. Craig, 'Introduction to Robotics (Mechanics and Control)', Addison-Wesley, 2nd Edition, 2004
2	John Craig," Introduction to Robotics ",4th Edition, Pearson , 2022.
3	Francis X. Govers, Artificial Intelligence for Robotics: Build intelligent robots that perform human tasks using AI techniques", 2018.

4	Richard D. Klafter, Thomas A. Chmielewski, Michael Negin, 'Robotics Engineering: An Integrated Approach', PHI Learning, New Delhi, 2009.
5	Yasmina Bestaoui Sebbane," Multi-UAV Planning and Task Allocation", CRC press, 2020.
6	K.S.Fu, R.C.Gonzalez and C.S.G.Lee, 'Robotics Control, Sensing, Vision and Intelligence', Tata McGraw Hill, 2nd Reprint, 2008.
7	Reza N.Jazar, 'Theory of Applied Robotics Kinematics, Dynamics and Control', Springer, 1st Indian Reprint, 2010.
8	Nicholas Odrey ,Mitchell Weiss , Mikell Groover and Roger Nagel," Industrial Robotics - Technology ,Programming and Applications",2nd Edition,2017.
9	Mikell. P. Groover, Michell Weis, Roger. N. Nagel, Nicolous G.Odrey, 'Industrial Robotics Technology, Programming and Applications ', McGraw Hill, Int 2012.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	**Programme Outcomes**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	2	2	2	1
CO2	2	1	2	2	2	1
CO3	2	1	2	2	2	1
CO4	2	1	2	2	2	1
CO5	2	1	2	2	2	1
CO	**2**	**1**	**2**	**2**	**2**	**1**

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: INTRODUCTION TO ROBOTICS	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: ROBOT KINEMATICS AND DYNAMICS	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: **R**OBOTICS CONTROL	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: ROBOT INTELLIGENCE AND TASK PLANNING	2	1either or	1(2)-CO3	1(2)-CO3	1either or (16)-CO4	-
Unit-V: INDUSTRIAL ROBOTICS	2	1either or	1(2)-CO3	1(2)-CO5 1either or (16)-CO5		-
Total Qns. Title:	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-

Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22212	**COMPUTER ARCHITECTURE AND PARALLEL PROCESSING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- Discuss the basic concepts and structure of computers.
- Explain the concepts of number representation and arithmetic operations.
- Explain different types of Memory architectures.
- Describe various parallel processing schemes and vector architecture.
- Summarize the Instruction execution stages and Memory hierarchy.

UNIT I	**INTRODUCTION TO COMPUTER ORGANIZATION**	**9**

Architecture and function of general computer system - Basic Operational Concepts, Bus Structures, Software Performance – Memory locations & addresses – Memory operations – Instruction and instruction sequencing – addressing modes – assembly language - System buses, Multi-bus organization

UNIT II	**DATA REPRESENTATION**	**9**

Signed number representation, fixed and floating point representations, character representation. Computer arithmetic - integer addition and subtraction, ripple carry adder, carry look-ahead adder - multiplication - shift-and-add, Booth multiplier, carry save multiplier - Division - non-restoring and restoring techniques, floating point arithmetic.

UNIT III	**PROCESSOR ARCHITECTURE AND CONTROL UNIT**	**9**

A Basic MIPS implementation – Building a Data path – Control Implementation Scheme – Hardwired control – micro programmed control - Pipelining – Pipelined data path and control – Handling Data Hazards & Control Hazards – Exceptions. Processor Architecture: Very Long Instruction Word (VLIW) Architecture, Digital Signal Processor Architecture, System on Chip (SoC) architecture, MIPS Processor and programming

UNIT IV	**PARALLEL PROCESSING**	**9**

Parallel processing challenges – Flyn's classification – Single Instruction Single Data (SISD), Multiple Instruction Multiple Data (MIMD), Single Instruction Multiple Data (SIMD), Single Program Multiple Data (SPMD), and Vector Architectures - Hardware multithreading – Multi-core processors and other Shared Memory Multiprocessors - Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message-Passing Multiprocessors.

UNIT V	**MEMORY & I/O SYSTEMS**	**9**

Memory Hierarchy – memory technologies – cache memory – measuring and improving cache performance – virtual memory, Translation Lookaside Buffers – Accessing I/O Devices – Interrupts– Direct Memory Access – Bus structure – Bus operation – Arbitration – Interface circuits – Universal Serial Bus.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course the student will be able to

CO1:	Identify the organization of computer and different opeartions, instruction formats, addressing modes and computer arithmetic
CO2:	Interpret the representation, manipulation of data on the computer and pipelining
CO3:	Explain processor architectures, multiprocessors and parallel processing

CO4:	Demonstrate the operations of computer arithmetic, the implementation schemes of processors and
CO5:	Outline the features of multiprocessors, memory hierarchy and I/O systems

REFERENCES:

1	David A. Patterson and John L. Hennessy, "Computer Organization and Design: The Hardware/Software Interface", Morgan Kaufmann / Elsevier, 5th Edition, 2014.
2	Carl Hamacher, ZvonkoVranesic, SafwatZaky and NaraigManjikian, "Computer Organizationand Embedded Systems", Tata McGraw Hill, 6th Edition, 2012.
3	William Stallings, "Computer Organization and Architecture — Designing for Performance",Pearson Education, 10th Edition, 2016.
4	John P. Hayes, "Computer Architecture and Organization", Tata McGraw Hill, 3rd Edition,2012.
5	John L. Hennessey and David A. Patterson, "Computer Architecture — A QuantitativeApproach", Morgan Kaufmann / Elsevier Publishers, 5th Edition, 2012.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	-	2	2	1	2
CO2	2	-	2	2	1	2
CO3	2	-	2	2	1	2
CO4	2	-	2	2	1	2
CO5	2	-	2	2	1	2
CO	**2**	**-**	**2**	**2**	**1**	**2**

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: Introduction To Computer Organization	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: Data Representation	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: Processor Architecture and Control Unit	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: Parallel Processing	2	1either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4	-	-
Unit-V: Memory & I/O Systems	2	1either or	1(2)-CO5	1(2)-CO5 1either or (16)-CO5	-	-
Total Qns.	10	5either or	7(2)	3(2) 5 either or (16)	-	-
Total Marks	20	80	14	86	-	-

Weightage	20%	80%	14%	86%	-	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22213	**VLSI DESIGN TECHNIQUES**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To understand the basics I-V characteristics of MOS transistor
- To introduce the VLSI design flow
- To Design combinational and sequential circuits
- To introduce testing of VLSI circuits
- To explore system design using Verilog HDL

UNIT I **CMOS TECHNOLOGY** **9**

MOS transistor, Ideal I–V characteristics, C–V characteristics, non-ideal I–V effects – CMOS Inverter and Pass transistor DC transfer characteristics – CMOS technologies, Layout design Rules – Stick Diagram – CMOS process enhancements– VLSI design Flow.

UNIT II **CIRCUIT DELAY,POWER, INTERCONNECT** **9**

Delay estimation – Logical effort and Transistor sizing – Power dissipation – Interconnect – Design margin –Reliability – Scaling – SPICE – Device models.

UNIT III **COMBINATIONAL AND SEQUENTIAL CIRCUIT DESIGN** **9**

Circuit families –Circuit Pitfalls – Sequencing static circuits, Max-min delay constraints, Time borrowing, Clock Skew – circuit design of latches and flip flops – synchronizers, Metastability, communication between asynchronous clock domains.

UNIT IV **CMOS TESTING** **9**

Need for testing – Testers, Text fixtures and test programs – Logic verification – Silicon debug principles –Manufacturing test – Design for testability – Boundary scan test.

UNIT V **SYSTEM DESIGN USING VERILOG HDL** **9**

Basic concepts- identifiers- gate primitives- gate delays- operators timing controls- procedural assignments-conditional statements- Design of combinational and sequential circuits using Data flow- structural gate level- switch level modeling and Behavioral modeling-Test benches. Advanced Verification Techniques.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course the student will be able to

CO1:	Explain the basics of CMOS technology, testing and circuit design
CO2:	Identify the methods to distribute clock and reduce power dissipation in CMOS circuits
CO3:	Execute the combinational and sequential circuits using Verilog HDL
CO4:	Analyze the characteristics of CMOS transistor and the methods to test the CMOS circuits
CO5:	Design combinational and sequential circuits

REFERENCES:

1	Weste and Harris: “CMOS VLSI DESIGN” 4th Edition, Pearson Education, 2013
2	Uyemura J.P: “Introduction to VLSI circuits and systems”, Wiley 2002.
3	D.APucknell & K.Eshraghian, “Basic VLSI Design”, 3rd Edition, PHI, 2003
4	Wayne Wolf, “Modern VLSI design”, 4th edition Pearson Education, 2009

5	M.J.S.Smith, "Application specific integrated circuits", 1st edition, Addison - Wesley Professional,1997
6	Ciletti, "Advanced Digital Design with the Verilog HDL", 2nd edition, Pearson Education2010
7	Samir Palnitkar "Verilog HDL a guide to digital design and Synthesis", Prentice Hall, 2ndedition, 2003
8	M. Morris Mano and Michael D. Ciletti, "Digital Design with an Introduction to the Verilog HDL, VHDL, and System Verilog", Sixth Edition, Pearson, 2018.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	**Programme Outcomes**					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	-	1	2	-	-
CO2	1	-	1	2	-	-
CO3	1	-	1	2	**2**	-
CO4	1	-	1	2	-	-
CO5	1	-	1	2	-	-
CO	1	-	1	2	**2**	-

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: CMOS TECHNOLOGY	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: CIRCUIT DELAY,POWER, INTERCONNECT	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: COMBINATIONAL AND SEQUENTIAL CIRCUIT DESIGN	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV:. CMOS TESTING	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO4		-
Unit-V: SYSTEM DESIGN USING VERILOG HDL	2	1either or	1(2)-CO3	1(2)-CO5	1either or (16)-CO5	-
Total Qns. Title: AE22213:VLSI DESIGN TECHNIQUES	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22214	INDUSTRIAL INTERNET OF THINGS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To understand the fundamentals of Internet of Things
- To learn about the basics of IOT protocols
- To build a small low cost embedded system using IoT
- To apply the concept of I0T in the real world scenario

UNIT I	INTRODUCTION AND ARCHITECTURE OF IoT	9

Introduction – Definition and characteristics of IoT – Physical and Logical Design of IoT - Communication models and APIs – Challenges in IoT - Evolution of IoT- Components of IoT - A Simplified IoT Architecture – Core IoT Functional Stack.

UNIT II	INDUSTRIAL IoT	9

IIoT-Introduction, Industrial IoT: Business Model and Reference Architecture: IIoT-Business Models, Industrial IoT- Layers: IIoT Sensing, IIoT Processing, IIoT Communication, IIoT Networking

UNIT III	IIOT ANALYTICS	9

Big Data Analytics and Software Defined Networks, Machine Learning and Data Science, Julia Programming, Data Management with Hadoop

UNIT IV	IOT SECURITY	9

Industrial IoT: Security and Fog Computing - Cloud Computing in IIoT, Fog Computing in IIoT, Security in IIoT

UNIT V	CASE STUDY	9

Industrial IOT- Application Domains: Oil, chemical and pharmaceutical industry, Applications of UAVs in Industries, Real case studies: Milk Processing and Packaging Industries, Manufacturing Industries

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course the student will be able to

CO1:	Describe the basic concepts and Architectures of Internet of Things, Machine learning, Big Data Analytics and Cloud Computing
CO2:	Describe the various layers of the Internet of Things and their relative importance
CO3:	Implement different IoT platforms and security measures
CO4:	Analyze the importance of Data Analytics in IoT
CO5:	Analyze the challenges, developments, and applications that are related to IoT

REFERENCES:

1	Industry 4.0: The Industrial Internet of Things", by Alasdair Gilchrist (Apress), 2017
2	"Industrial Internet of Things: Cybermanufacturing Systems"by Sabina Jeschke, ChristianBrecher, Houbing Song, Danda B. Rawat (Springer), 2017
3	Hands-On Industrial Internet of Things: Create a powerful Industrial IoT by Giacomo Veneri, Antonio Capasso, Packt, 2018.
4	"Industrial IoT Challenges, Design Principles, Applications, and Security," by Ismail Butun, 2020.
5	Industrial Internet of Things,Technologies, Design, and Applications, Sudan Jha, Usman Tariq,Gyanendra Prasad Joshi, Vijender Kumar Solanki, 2022.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	-	-	1	-

CO2	2	2	-	-	1	-
CO3	2	2	1	1	1	-
CO4	2	2	1	1	1	1
CO5	2	2	1	1	1	1
CO	2	2	1	1	1	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: INTRODUCTION AND ARCHITECTURE OF IoT	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: INDUSTRIAL IoT	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: IIOT ANALYTICS	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV:. IOT SECURITY	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO4	-	-
Unit-V: CASE STUDY	2	1either or	1(2)-CO3	1(2)-CO5	1either or (16)-CO5	-
Total Qns. Title:	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

SEMESTER II, PROFESSIONAL ELECTIVE III

AE22221	**QUANTUM COMPUTING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**
COURSE OBJECTIVES:					
• To introduce the building blocks of Quantum computers and highlight the paradigm changebetween conventional computing and quantum computing					
• To understand the Quantum state transformations and the algorithms					
• To understand entangled quantum subsystems and properties of entangled states					
• To explore the applications of quantum computing					
UNIT I	**QUANTUM BUILDING BLOCKS**				**9**

The Quantum Mechanics of Photon Polarization, Single-Qubit Quantum Systems, Quantum State Spaces, Entangled States, Multiple-Qubit Systems, Measurement of Multiple-Qubit States, EPR Paradox and Bell's Theorem, Bloch sphere		
UNIT II	**QUANTUM STATE TRANSFORMATIONS**	**9**
Unitary Transformations, Quantum Gates, Unitary Transformations as Quantum Circuits, Reversible Classical Computations to Quantum Computations, Language for Quantum Implementations.		
UNIT III	**QUANTUM ALGORITHMS**	**9**
Computing with Superpositions, Quantum Subroutines, Quantum Fourier Transformations, Shor's Algorithm and Generalizations, Grover's Algorithm and Generalizations		
UNIT IV	**ENTANGLED SUBSYSTEMS AND ROBUST QUANTUM COMPUTATION**	**9**
Quantum Subsystems, Properties of Entangled States, Quantum Error Correction, Graph states and codes, CSS Codes, Stabilizer Codes, Fault Tolerance and Robust Quantum Computing		
UNIT V	**QUANTUM INFORMATION PROCESSING**	**9**
Limitations of Quantum Computing, Alternatives to the Circuit Model of Quantum Computation, Quantum Protocols, Building Quantum, Computers, Simulating Quantum Systems, Bell states. Quantum teleportation. Quantum Cryptography, no cloning theorem		
TOTAL:45 PERIODS		

COURSE OUTCOMES:	
Upon the completion of course, students will be able to	
CO1:	Explain the basic principles and algorithms of quantum computing
CO2:	Describe quantum subsystems and quantum protocols
CO3:	Develop several algorithms for quantum computing
CO4:	Solve the problem of Fault Tolerance and Robust Quantum Computing
CO5:	Analyze and simulate quantum-based systems

REFERENCES:

1.	John Gribbin, Computing with Quantum Cats: From Colossus to Qubits, 2021
2.	William (Chuck) Easttom, Quantum Computing Fundamentals, 2021
3.	Parag Lala, Quantum Computing, 2019
4.	Eleanor Rieffel and Wolfgang Polak, QUANTUM COMPUTING A Gentle Introduction, 2011
5.	Nielsen M. A., Quantum Computation and Quantum Information, Cambridge UniversityPress.2002
6.	Benenti G., Casati G. and Strini G., Principles of Quantum Computation and Information, Vol. I:Basic Concepts, Vol II: Basic Tools and Special Topics, World Scientific. 2004
7.	Pittenger A. O., An Introduction to Quantum Computing Algorithms 2000

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	2	1	-	-	-
CO2	2	2	1	-	-	-
CO3	2	-	1	1	1	-
CO4	2	-	1	1	1	1
CO5	2	-	1	1	1	1
CO	2	2	1	1	1	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: QUANTUM BUILDING BLOCKS	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: QUANTUM STATE TRANSFORMATIONS	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: QUANTUM ALGORITHMS	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: ENTANGLED SUBSYSTEMS AND ROBUST QUANTUM COMPUTATION.	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO4	-	-
Unit-V: QUANTUM INFORMATION PROCESSING	2	1either or	1(2)-CO3	1(2)-CO5	1either or (16)-CO5	-
Total Qns. Title:	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

CU22222	**VLSI FOR WIRELESS COMMUNICATION**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To understand the concepts of basic wireless communication concepts.
- To study the parameters in receiver and low noise amplifier design.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of transmitters and power amplifiers in wireless communication

UNIT I **COMMUNICATION CONCEPTS** **9**

Introduction – Overview of Wireless systems – Standards – Access Methods – Modulation schemes – Classical channel – Wireless channel description – Path loss – Multipath fading –Standard Translation

UNIT II **RECEIVER ARCHITECTURE & LOW NOISE AMPLIFIERS** **9**

Receiver front end – Filter design – Non-idealities – Design parameters – Noise figure & Inputintercept point. LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedancematching & Core amplifier

UNIT III	MIXERS	9
Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain — Distortion — Noise - A Complete Active Mixer. Switching Mixer — Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer		
UNIT IV	**FREQUENCY SYNTHESIZERS**	**9**
PLL — Phase detector — Dividers — Voltage Controlled Oscillators — LC oscillators — Ring Oscillators – Phase noise – Loop filters & design approaches – A complete synthesizer design example (DECT) – Frequency synthesizer with fractional divider		
UNIT V	**TRANSMITTER ARCHITECTURES & POWER AMPLIFIERS**	**9**
Transmitter back end design – Quadrature LO generator – Power amplifier design. case study: GSM		
		TOTAL : 45 PERIODS

COURSE OUTCOMES:	
At the end of the course, the students will be able to:	
CO1:	Describe the basic wireless communication concepts.
CO2:	Explain the parameters in receiver and design a low noise amplifier
CO3:	Apply knowledge on various types of mixers designed for wireless communication.
CO4:	Analyze the Phase Lock Loop and Voltage Controlled Oscillator.
CO5:	Design the transmitters and the power amplifiers for wireless communication.

REFERENCES:	
1.	Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
2.	B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.
3.	Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.
4.	Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI wireless design — Circuits & Systems", Kluwer Academic Publishers, 2000.
5.	J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer AcademicPub., 1997.
6.	Thomas H.Lee, "The Design of CMOS Radio — Frequency Integrated Circuits", Cambridge University Press ,2003.
7.	Prashant Ranjan, Ram Shringar Rao, Krishna Kumar, Pankaj Sharma, "Wireless Communication: Advancements and Challenges", CRC Press, 2022.
8.	Forouhar Farzaneh, Ali Fotowat, Mahmoud Kamarei, Ali Nikoofard, Mohammad Elmi, "Introduction to Wireless Communication Circuits", River Publishers, 2018.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	2	1	2	1	2
CO2	2	2	2	2	1	2
CO3	2	2	1	2	2	2
CO4	2	2	2	2	2	1
CO5	2	2	1	1	2	2
CO	2	2	1.4	1.8	1.6	1.8

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: COMMUNICATION CONCEPTS	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: RECEIVER ARCHITECTURE & LOW NOISE AMPLIFIERS	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: MIXERS Unit-IV: FREQUENCY SYNTHESIZERS	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-V: TRANSMITTER ARCHITECTURES & POWER AMPLIFIERS	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO4	1either or (16)-CO4	-
Unit-I: COMMUNICATION CONCEPTS Unit-II: RECEIVER ARCHITECTURE & LOW NOISE AMPLIFIERS	2	1either or	1(2)-CO3	1(2)-CO5 1either or (16)-CO5		-
Unit-III: MIXERS	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22222	**MICRO ELECTRO MECHANICAL SYSTEMS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To understand the operation of sensors and actuators
- To understand the operation of major classes of MEMS devices/systems
- To give the fundamentals of standard micro fabrication techniques and processes
- To understand the unique demands, environments and applications of MEMS devices
- To understand RF MEMS, Bio MEMS and MOEMS

UNIT I	INTRODUCTION TO MEMS	9
Intrinsic Characteristics of MEMS – Energy Domains and Transducers- Sensors and Actuators – Introduction to Micro fabrication - Silicon based MEMS processes – New Materials – Review of Electrical and Mechanical concepts in MEMS – Semiconductor devices – Stress and strain analysis – Flexural beam bending- Torsional deflection		
UNIT II	**SENSORS AND ACTUATORS**	**9**
Electrostatic sensors – Parallel plate capacitors – Applications – Interdigitated Finger capacitor- Piezoresistive sensors – Piezoresistive sensor materials - piezoelectric effects – piezoelectric materials-Stress analysis of mechanical elements – Thermal Sensing and Actuation – Thermal expansion – Thermal couples – Thermal resistors – Thermal Bimorph - Applications – Magnetic Actuators – Micromagnetic components. Advanced machining processes		
UNIT III	**MICROMACHING**	**9**
Silicon Anisotropic Etching – Anisotrophic Wet Etching – Dry Etching of Silicon – Plasma Etching – Deep Reaction Ion Etching (DRIE) – Isotropic Wet Etching – Gas Phase Etchants – Case studies – Basic surface micro machining processes – Structural and Sacrificial Materials – Acceleration of sacrificial Etch – Striction and Antistriction methods – LIGA Process - Assembly of 3D MEMS – Foundry process		
UNIT IV	**POLYMER AND OPTICAL MEMS**	**9**
Polymers in MEMS – SU-8, PMMA, PDMS, Langmuir – Blodgett Films, Micro System fabrication – Photolithography – Ion implantation- Diffusion – Oxidation – Chemical vapour deposition – Etching- Optical MEMS – Lenses and Mirrors – Actuators for Active Optical MEMS		
UNIT V	**OVERVIEW OF MEMS AREAS**	**9**
Bonding techniques for MEMS : Surface bonding , Anodic bonding , Silicon - on - Insulator , wire bonding , Sealing — Assembly of micro systems- RF MEMS - switches, active and passive components, Bio MEMS - Microfluidics, Digital Micro fluidics, Ink jet printer,- MOEMS and Multifunctional Systems , optical switch, optical cross-connect, tunable VCSEL, micro bolometers		
		TOTAL : 45 PERIODS

SUGGESTED ACTIVITIES:

1. Expose the students to occupational environment related to semiconductor devices and MEMS
2. Create opportunity for acquiring practical skills of various field instruments in the area of MEMS devices
3. Manage the issues arising during the execution of projects related to MEMS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Explain the working principles of micro sensors and actuators
CO2:	Summarize the materials used for fabrication of micro machines
CO3:	Design of microsystems based on scaling laws
CO4:	Apply the principles of standard micro fabrication techniques
CO5:	Analyse the design and fabrication challenges in RF, Bio, and MOEMS systems

REFERENCES:

1.	Stephen D Senturia, 'Microsystem Design', Springer Publication, 2000
2.	Chang Liu, 'Foundations of MEMS', Pearson Education Inc., 2012
3.	Marc J. Madou, 'Fundamentals of Microfabrication: The Science of Miniaturization', Second Edition , 2002.
4.	Nadim Maluf," An Introduction to Micro Electro Mechanical System Design", Artech House, 2000.
5.	Mohamed Gad-el-Hak, editor, " The MEMS Handbook", CRC press Baco Raton,2001.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	-	2	1	-	-
CO2	2	-	2	1	-	-
CO3	2	2	2	2	1	-
CO4	2	2	2	2	1	-
CO5	2	2	2	2	1	1
CO	2	2	2	1.6	1	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: INTRODUCTION TO MEMS	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: SENSORS AND ACTUATORS	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: MICRO MACHING	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: POLYMER AND OPTICAL MEMS	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO4	-	-
Unit-V: OVERVIEW OF MEMS AREAS	2	1either or	1(2)-CO3	1(2)-CO5	1either or (16)-CO5	-
Total Qns. Title:	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22223	**CAD FOR VLSI DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To introduce the VLSI design methodologies and design methods.
- To introduce data structures and algorithms required for VLSI design.
- To study algorithms for partitioning and placement.

• To study algorithms for floor planning and routing.		
• To study algorithms for modelling, simulation and synthesis.		
UNIT I	**INTRODUCTION**	**9**
Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI Design Cycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles – Reviewof VLSI Design Automation Tools		
UNIT II	**DATA STRUCTURES AND BASIC ALGORITHMS**	**9**
Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization		
UNIT III	**ALGORITHMS FOR PARTITIONING AND PLACEMENT**	**9**
Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction –Partitioning – Placement – Placement Algorithms		
UNIT IV	**ALGORITHMS FOR FLOOR PLANNING AND ROUTING**	**9**
Floorplanning – Problem Formulation – Floorplanning Algorithms – Routing – Area Routing –Global Routing – Detailed Routing		
UNIT V	**MODELLING, SIMULATION AND SYNTHESIS**	**9**
Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.		
		TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Describe the different data structures and algorithms required for VLSI design
CO2:	Discuss various VLSI design methodologies.
CO3:	Compare various VLSI design algorithms
CO4:	Develop algorithms for partitioning, placement, floor planning and routing
CO5:	Design algorithms for modelling, simulation and synthesis

REFERENCES:

1.	Sabih H. Gerez, "Algorithms for VLSI Design Automation", Second Edition, Wiley-India, 2017
2.	Naveed a. Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, Springer,2017
3.	Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, "Handbook of Algorithms forPhysical Design Automation, CRC Press, 1st Edition, 2.
4.	N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
5.	Steven M Rubin, Computer Aids for VLSI Design, Third edition, R. L. Ranch Press, 2009.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	-	-	1	2	-	-
CO2	-	-	1	2	-	-
CO3	-	-	1	2	-	-
CO4	-	-	1	2	-	
CO5	-	-	1	2	2	-
CO	**-**	**-**	**1**	**2**	**2**	**-**

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: INTRODUCTION	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: DATA STRUCTURES AND BASIC ALGORITHMS	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: ALGORITHMS FOR PARTITIONING AND PLACEMENT	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV:. ALGORITHMS FOR FLOOR PLANNING AND ROUTING	2	1either or	1(2)-CO3	1(2)-CO3	1either or (16)-CO4	-
Unit-V: MODELLING, SIMULATION AND SYNTHESIS	2	1either or	1(2)-CO3	1(2)-CO5 1either or (16)-CO5		-
Total Qns. Title: AE22223-CAD FORVLSI DESIGN	1	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

AE22224	**HARDWARE SECURE COMPUTING**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- Describe the fundamental principles in Data security
- Discuss the watermarking algorithms and its usage
- Explain the physical attacks and Modular arithmetic security methods
- Describe the memory based attacks and vulnerabilities using deceptive mechanisms
- Discuss the methods of FPGA implementation of cryptographic algorithms

UNIT I	**INTRODUCTION TO CRYPTO ALGORITHMS**	**9**

Cryptography basics, Cryptographic algorithms - Symmetric Key algorithms, Public Key algorithms and Hash Algorithms, Data Encryption Standards, Advanced Encryption Standards, RSA, BowFish

UNIT II	**HARDWARE SECURITY**	**9**

Need for Hardware Security, Computer Memory and storage, Bus and Interconnection, I/O and Network Interface, CPU; Side channel Analysis: Power Analysis Attack, Timing Attack, Fault attack. Counter measures of Side Channel Attack, Secure Hardware Intellectual Properties		
UNIT III	**PHYSICAL ATTACKS AND MODULAR EXPONENTIATION**	**9**
Physical Attacks (PA) Basics, Physical Attacks and Countermeasures, Building Secure Systems, Modular Exponentiation (ME) Basics, ME in Cryptography, ME Implementation and Vulnerability, Montgomery Reduction		
UNIT IV	**ATTACKS AND COUNTER MEASURES**	**9**
Introduction to Side Channel Attacks, Memory Vulnerabilities and Cache Attacks, Power Analysis, More Attacks and Countermeasures, Modified Modular Exponentiation, Hardware Trojan (HT) and Trusted IC, Hardware Trojan Taxonomy, Hardware Trojan Detection Overview, Hardware Trojan Detection Methods, Trusted IC Design with HT Prevention		
UNIT V	**EMERGING TECHNOLOGIES**	**9**
FPGA Implementation of Crypto algorithms, Vulnerabilities and Countermeasures in FPGA Systems, Role of Hardware in Security and Trust, Physical Unclonable Functions (PUF) Basics, Reliability, Trust Platform Modules		
		TOTAL:45 PERIODS
COURSE OUTCOMES:		
At the end of the course, the students will be able to:		
CO1:	Infer the basics concepts of Cryptography	
CO2:	Employ the mechanism of Data Integrity protection mechanisms	
CO3:	Analyze the counter measures for physical attacks and the use of Modularexponentiation	
CO4:	Frame appropriate counter measures for various attacks	
CO5:	Solve the challenges in Realization using VLSI implementations exponentiation(K2)	
REFERENCES:		
1.	Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, Hardware Security: Design, Threats,and Safeguards, CRC Press,2014	
2.	Tehranipoor, Mohammad, Wang, Introduction to Hardware Security and Trust, Springer,2011	
3.	Ted Huffmire, Handbook of FPGA Design Security, Springer,2010	
4.	Stefan Mangard, Elisabeth Oswald, Thomas Popp, Power Analysis Attacks - Revealing theSecrets of Smart Cards, Springer,2007	
5.	Doug Stinson, Cryptography Theory and Practice, CRC Press,2018	

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	2	2	2	2
CO2	2	1	2	2	2	2
CO3	2	1	2	2	2	2
CO4	2	1	2	2	2	2
CO5	2	1	2	2	2	2
CO	2	1	2	2	2	2

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: Introduction To Crypto Algorithms	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: Hardware Security	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: Physical Attacks And Modular Exponentiation	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV:. Attacks And Counter Measures	2	1either or	1(2)-CO3	1(2)-CO3	1either or (16)-CO4	-
Unit-V: Emerging Technologies	2	1either or	1(2)-CO3	1(2)-CO5 1either or (16)-CO5		-
Total Qns. Title: AE22224 Hardware Secure Computing	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

Weightage for COs

	CO1	CO2	CO3	CO4	CO5
Total Marks	20	20	20	20	20
Weightage	20%	20%	20%	20%	20%

SEMESTER III, PROFESSIONAL ELECTIVE IV

AE22311	**MODELING AND SYNTHESIS WITH HDL**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To know the basic language features of Verilog HDL and its the role in digital logic design.
- To know the behavioral modeling of combinational and sequential circuits.
- To know the behavioral modeling of algorithmic state machines.
- To know the synthesis of combinational and sequential descriptions.
- To know the architectural features of programmable logic devices.

UNIT I	**INTRODUCTION TO LOGIC DESIGN WITH VERILOG**	**7**

Overview of Digital Design with Verilog HDL - Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a

simulation, design block, stimulus block - Basic Concept- Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing. Tasks and Functions.		
UNIT II	**LEVELS OF MODELING**	**12**
Gate-Level Modeling : Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. Dataflow Modeling: Continuous assignments, delay specification, expressions, operators, operands, operator types. Behavioral Modeling: Structured procedures, initial and always, blocking and nonblocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.		
UNIT III	**DESIGN OF DIGITAL LOGIC USING HDL**	**12**
Design of combinational logic: adders, multiplexers, de-multiplexers, encoders and decoders, comparators, multipliers - Design of Sequential logic: Flip-flops, synchronous and Asynchronous counters, shift registers, Universal shift register, FSM and LFSR.(Using various Levels of Modeling)		
UNIT IV	**LOGIC SYNTHESIS AND DESIGN FLOW**	**7**
Logic Synthesis with verilog HDL-Synthesis Design flow, RTL and Test Bench Modeling Techniques and Timing and Path Delay Modeling, Timing Checks, Switch Level Modeling, case study : synthsizable FIFO model.		
UNIT V	**PROGRAMMABLE LOGIC DEVICES**	**7**
Programmable logic devices, storage devices, programmable logic array programmable array logic, programmability of PLDs CPLDs.		
TOTAL: 45 PERIODS		
PRACTICAL EXERCISES:		**30 PERIODS**
1. Design Using VHDL Or Verilog Using HDL Languages of . I. Combinational Circuits namely 8:1 Mux/Demux, Full Adder, 8-Bit Magnitude Comparator, Encoder/Decoder, Priority Encoder. II. Sequential Circuits namely D-FF, 4-Bit Shift Registers (SISO, SIPO, PISO, Bidirectional), 3- Bit Synchronous Counters.		
2. I. Test Vector Generation and Timing Analysis of Sequential and Combinational Logic Design for exercise (1) above. II. Synthesis, P&R And Post P&R Simulation of the Components Simulated In (1) Above.		
3. FPGA Implementation of PCI Bus & Arbiter. Verifying Design Functionality Using Either Chipscope Feature (Xilinx) /the Signal Tap Feature (Altera)/Other Equivalent Feature . Invoke the PLL And Demonstrate the Use of the PLL Module for Clock Generation in FPGAs.		
TOTAL PERIODS:75		
COURSE OUTCOMES:		
At the end of the course, the students will be able to:		
CO1:	Explain the basics of digital logic design using Verilog HDL.	
CO2:	Illustrate various levels of modelling.	
CO3:	Design combinational and sequential logic using various levels of modeling in HDL.	
CO4:	Explain logic synthesis and design flow.	
CO5:	Explain the architectural features of programmable logic devices.	
REFERENCES:		
1.	Michael D Ciletti - Advanced Digital Design with the VERILOG HDL, 2nd Edition, PHI, 2009.	
2.	Charles H. Roth Jr., Lizy K. John, “Digital design using HDL”, Cengage Learning, Third Edition, 2016.	
3.	Suman Lata Tripathi, Sobhit Saxena, Sanjeet K. Sinha, “Digital VLSI Design and Simulation with Verilog”, John Wiley & Sons., 2022.	
4.	Z Navabi - Verilog Digital System Design, 2nd Edition, McGraw Hill, 2005.4	

5.	Stephen Brown and Zvonko Vranesic - Fundamentals of Digital Logic with Verilog, 2nd Edition, TMH, 2008.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	-	2	1	2	1
CO2	2	-	2	1	2	1
CO3	2	-	2	1	2	1
CO4	2	-	2	1	2	1
CO5	2	-	2	1	2	1
CO	2	-	2	1	2	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: Introduction to Logic Design with Verilog	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: Levels of Modeling	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: Design of Digital Logic using HDL	2	1either or	1(2)-CO3	1(2)-CO3	1either or (16)-CO3	-
Unit-IV: Logic Synthesis and Design Flow	2	1either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4	-	-
Unit-V: Programmable Logic Devices	2	1either or	2(2)-CO5	1either or (16)-CO5		-
Total Qns. Title: AE22311MODELING AND SYNTHESIS WITH HDL	10	5either or	8(2)	2(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	16	68	16	-
Weightage	20%	80%	16%	68%	16%	-

MX22313	DEEP LEARNING	L	T	P	C
		3	0	2	4

COURSE OBJECTIVES:

- To develop and Train Deep Neural Networks.
- To develop a CNN for object detection and recognition.
- To build and train RNNs, to solve real-world problems.
- To study the structure of LSTM and GRU and the differences between them
- To design Auto Encoders for Image Processing.

UNIT I	INTRODUCTION TO DEEP LEARNING	9
Review of Neural Networks- Building Blocks of Neural Network. Multilayer Perceptron, Back-propagation algorithm and its variants Stochastic gradient decent, Optimizers. Activation Functions. Loss Functions, Data Pre-processing for neural networks, Overfitting and Underfitting. Hyperparameters, Deep networks		
UNIT II	**CONVOLUTIONAL NEURAL NETWORK**	**9**
CNN. Architecture- Input Layers, Convolution Layers. Pooling Layers. Dense Layers, Filters and Feature Maps, Dropout Layers and Regularization, Batch Normalization. Various Activation Functions. Various Optimizers. Popular CNN Architectures: LeNet, AlexNet, VGG16, ResNet, UNet		
UNIT III	**TRANSFER LEARNING & SEQUENCE MODELLING**	**9**
Transfer Learning with Image Data. RCNN, Fast R-CNN, Faster R-CNN, Mask-RCNN, YOLO. Recurrent Neural Networks, Bidirectional RNNs (BRNN). Long Short-Term Memory (LSTM). Bi-directional LSTM. Sequence-to-Sequence Models (Seq2Seq). Gated recurrent unit GRU.		
UNIT IV	**DEEP REINFORCEMENT & UNSUPERVISED LEARNING**	**9**
About Deep Reinforcement Learning. Q-Learning. Deep Q-Network (DQN). Policy Gradient Methods. Actor-Critic Algorithm. About Autoencoding. Convolutional Auto Encoding. Variational Auto Encoding. Generative Adversarial Networks.		
UNIT V	**APPLICATIONS OF DEEP LEARNING**	**9**
Autoencoders for Feature Extraction. Auto Encoders for Classification. Denoising Autoencoders. Sparse Autoencoders. Case studies-Deep Neural network for Medical image segmentation		
		TOTAL :45 PERIODS
PRACTICAL EXERCISES:		**30 PERIODS**
LIST OF EXPERIMENTS		
1. Implement a perceptron in TensorFlow/Keras Environment.		
2. Implement a Feed-Forward Network in TensorFlow/Keras. for signal / Image data.		
3. Implement an Image Classifier using CNN in TensorFlow/Keras for abnormal detection.		
4. Implement a Transfer Learning concept for medical Image Classification.		
5. Implement an Autoencoder in TensorFlow/Keras and improve the deep learning model by tuning hyper parameters		
6. Implement a Simple LSTM using TensorFlow/Keras		
7. Implement a classifier in Recurrent Neural network.		
		TOTAL :75 PERIODS
COURSE OUTCOMES:		
At the end of the course, the students will be able to:		
CO1:	Realize neural network for data preprocessing and feature extraction.	
CO2:	Understand CNN architecture for object detection.	
CO3	Understand transfer learning and recurrent networks	
CO4:	Analyze the Deep Reinforcement & Unsupervised Learning networks	
CO5:	Apply deep learning network for Feature Extraction and Classification..	
REFERENCES:		
1.	Deep Learning A Practitioner's Approach Josh Patterson and Adam Gibson O'Reilly Media, Inc.2017.	
2.	Learn Keras for Deep Neural Networks, Jojo Moolayil, Apress,2018.	
3.	Deep Learning Projects Using TensorFlow 2, Vinita Silaparasetty, Apress, 2020.	
4.	Deep Learning with Python, François Chollet, Manning Shelter Island,2017.	
5.	Pro Deep Learning with TensorFlow, Santanu Pattanayak, Apress,2017.	
6.	Ian Goodfellow, YoshuaBengio and Aaron Courville, " Deep Learning", MIT Press, 2017.	
7.	Umberto Michelucci "Applied Deep Learning. A Case-based Approach to Understanding Deep Neural Networks" Apress, 2018.	

8.	https://nptel.ac.in/courses/106106184

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	-	-	2	1
CO2	1	-	-	1	2	1
CO3	1	-	-	1	2	1
CO4	1	-	-	2	2	1
CO5	1	-	-	2	2	1
CO	1	-	-	1.5	2	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: INTRODUCTION TO DEEP LEARNING	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: CONVOLUTIONAL NEURAL NETWORK	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: TRANSFER LEARNING & SEQUENCE MODELLING	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: DEEP REINFORCEMENT & UNSUPERVISED LEARNING	2	1either or	1(2)-CO4	1(2)-CO4	-	1either or (16)-CO4
Unit-V: APPLICATIONS OF DEEP LEARNING	2	1either or	1(2)-CO5	1(2)-CO5	1either or (16)-CO5	-
Total Qns.	10	5either or	7(2)	3(2) 3 either or (16)	1 either or (16)	1 either or (16)
Total Marks	20	80	14	54	16	16
Weightage	20%	80%	14%	54%	16%	16%

AE22312	DIGITAL IMAGE PROCESSING	L	T	P	C
		3	0	2	4

COURSE OBJECTIVES:

- To understand the image fundamentals and mathematical transforms necessary for image

processing and to study the image enhancement techniques.		
• To understand the image segmentation and representation techniques.		
• To understand how image are analyzed to extract features of interest.		
• To introduce the concepts of image registration and image fusion.		
UNIT I	**FUNDAMENTALS OF DIGITAL IMAGE PROCESSING**	**9**
Elements of visual perception, brightness, contrast, hue, saturation, match band effect, 2D image transforms - DFT, DCT, KLT, and SVD. Image enhancement in spatial and frequency domain, Morphological image processing, Fundamentals of Color Image Processing.		
UNIT II	**FEATURE EXTRACTION**	**9**
First and second order edge detection operators, Phase congruency, Localized feature extraction detecting image curvature, shape features Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Run length features, Fractal model-based features, Gabor filter, wavelet features.		
UNIT III	**SEGMENTATION**	**9**
Edge detection, Thresholding, Region growing, Fuzzy clustering, Watershed algorithm, Active contour methods, Model based segmentation, Atlas based segmentation, Wavelet based Segmentation methods.		
UNIT IV	**IMAGE REGISTRATION**	**9**
Registration- Pre-processing, Feature selection-points, lines, regions and templates Feature Correspondence-Point pattern matching, Line matching, region matching Template matching. Transformation functions-Similarity transformation and Affine Transformation. Resampling-Nearest Neighbour and Cubic Splines.		
UNIT V	**IMAGE FUSION**	**9**
Image Fusion-Overview of image fusion, pixel fusion, Multiresolution based fusion discrete wavelet transforms, Curvelet transform. Region based fusion.		
TOTAL: 45 PERIODS		
PRACTICAL EXERCISES:		**30 PERIODS**
LIST OF EXPERIMENTS		
• Wavelet and DCT based Image Compression		
• Geometrical transformations and Interpolation of Images		
• Edge Detection using Canny edge detector		
• Region based, threshold based and Watershed Segmentation		
• Image filtering using DFT		
• Texture, Gabor and Wavelet Feature Extraction		
• Image fusion using Wavelets		
TOTAL:75 PERIODS		
COURSE OUTCOMES:		
At the end of the course, the students will be able to:		
CO1:	State the fundamental concepts of image processing.	
CO2:	Describe the image analysis techniques in the form of image segmentation.	
CO3:	Implement various feature extraction techniques.	
CO4:	Demonstrate the concepts of image registration.	
CO5:	Implement image fusion concepts.	
REFERENCES:		
1.	John C.Russ, F. Brent Neal , "The Image Processing Handbook", CRC Press, 2017.	
2.	Mark Nixon, Alberto Aguado, "Feature Extraction and Image Processing", Academic Press,2008.	
3.	Rafael C. Gonzalez, Richard E. Woods, , Digital Image Processing', Pearson, Education, Inc., Fourth Edition, 2018.	
4.	Anil K. Jain, Fundamentals of Digital Image Processing', Pearson Education, Inc., 2002.	

5.	Rick S.Blum, Zheng Liu," Multisensor image fusion and its Applications", Taylor & Francis,2006.
6.	Gopi E.S, "Digital Image Processing Using MATLAB", Scitech Publications (India) Pvt Ltd, 2015.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	2	1	2	1	1
CO2	2	2	1	2	1	1
CO3	2	2	1	2	1	1
CO4	2	2	1	2	1	1
CO5	2	2	1	2	1	1
CO	2	2	1	2	1	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: FUNDAMENTALS OF DIGITAL IMAGE PROCESSING	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: FEATURE EXTRACTION	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: SEGMENTATION	2	1either or	1(2)-CO3	1(2)-CO3	1either or (16)-CO3	-
Unit-IV: IMAGE REGISTRATION	2	1either or	1(2)-CO4	1(2)-CO4	1either or (16)-CO4	-
Unit-V: IMAGE FUSION	2	1either or	1(2)-CO5	1(2)-CO5	1either or (16)-CO5	-
Total Qns. Title:AE22312 DIGITAL IMAGE PROCESSING	10	5either or	7(2)	3(2) 2 either or (16)	3 either or (16)	-
Total Marks	20	80	14	38	48	-
Weightage	20%	80%	14%	38%	48%	-

MX22203	**MACHINE LEARNING TECHNIQUES**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To understand the concepts and mathematical foundations of machine learning and types of problems tackled by machine learning

• To explore the different supervised learning techniques including ensemble methods		
• To learn different aspects of unsupervised learning and reinforcement learning		
• To learn the role of probabilistic methods for machine learning		
• To understand the basic concepts of neural networks and deep learning		
UNIT I	**MATHEMATICAL BACKROUND**	**9**
Machine Learning–Types of Machine Learning –Machine Learning process, Mathematical Foundations – Linear Algebra – Arithmetic of matrices, Norms, Eigen decomposition, Singular value decomposition. Probability theory – probability distribution, decision theory.		
UNIT II	**SUPERVISED LEARNING**	**9**
Introduction-Discriminative and Generative Models -Linear Regression - Least Squares -Under-fitting / Overfitting -Cross-Validation – Lasso Regression- Classification - Logistic Regression- Gradient Linear Models -Support Vector Machines –Kernel Methods -Instance based Methods - K-Nearest Neighbors - Tree based Methods –Decision Trees –CART - Ensemble Methods –Random Forest.		
UNIT III	**UNSUPERVISED LEARNING**	**9**
Introduction - Clustering Algorithms -K – Means – Hierarchical Clustering - spectral clustering-Cluster Validity - Dimensionality Reduction –Principal Component Analysis, Independent Components Analysis.		
UNIT IV	**BAYESIAN LEARNING**	**9**
Introduction -Naïve Bayes Algorithm -Maximum Likelihood -Maximum Apriori -Bayesian Belief Networks -Probabilistic Modelling of Problems - Bayesian Linear Regression.		
UNIT V	**NEURAL NETWORKS AND DEEP LEARNING**	**9**
Artifitial Neural Networks –- Perceptron – Multi-layer Perceptron — Back Propagation –Activation function and Loss Functions- Introduction to Deep Learning– Convolution Neural Networks – Recurrent Neural Networks – case study.		
TOTAL: 45 PERIODS		
PRACTICAL EXERCISES:		**30 PERIODS**
LIST OF EXPERIMENTS		
1. Implement a Linear Regression model and tune the model's hyperparameters.		
2. Implement a binary classification model determine the model's effectiveness with different classification metrics.		
3. Classify the normal and abnormal bio signals with Nearest Neighbor classifier.		
4. Analyze the training and validation results of the classifier. Detect and fix a common training problem.		
5. Implement the k-means algorithm using https://archive.ics.uci.edu/ml/datasets/Codon+usage dataset		
6. Implement the Naïve Bayes Classifier using https://archive.ics.uci.edu/ml/ datasets/ Gait+ Classification dataset		
7. Implement the convolutional neural network for feature extraction and classification of medical images.		
TOTAL : 75 PERIODS		
COURSE OUTCOMES:		
At the end of the course, the students will be able to:		
CO1:	Explain the mathematical and statistical prospective of machine learning algorithms	
CO2:	Design a Decision tree and Random forest for an application	
CO3:	Implement Probabilistic Discriminative and Generative algorithms for an application and analyze the results	

CO4:	Implement Clustering algorithms and HMM for different types of applications
CO5:	Implement neural network and deep learning algorithms for suitable applications

REFERENCES:

1	Stephen Marsland, "Machine Learning: An Algorithmic Perspective", Chapman & Hall/CRC, 2nd Edition, 2014.
2	Ethem Alpaydin, "Introduction to Machine Learning", Third Edition, Adaptive Computation and Machine Learning Series, MIT Press, 2014..
3	Tom M Mitchell, "Machine Learning", McGraw Hill Education, 2013.
4	Shai Shalev-Shwartz and Shai Ben-David, "Understanding Machine Learning: From Theory to Algorithms", Cambridge University Press, 2015.
5	Christopher Bishop, "Pattern Recognition and Machine Learning", Springer, 2007.
6	Hal Daumé III, "A Course in Machine Learning", 2017 (freely available online).
7	Trevor Hastie, Robert Tibshirani, Jerome Friedman, "The Elements of Statistical Learning", Springer, 2009 (freely available online).
8	Aurélien Géron , Hands-On Machine Learning with Scikit-Learn and TensorFlow: Concepts, Tools, and Techniques to Build Intelligent Systems 2nd Edition, o'reilly, (2017).
9	Kevin P Murphy, Machine Learning: A Probabilistic Perspective,2nd Edition, MIT Press, 2022.
10	Csaba Szepesvari, Algorithms for Reinforcement Learning (Synthesis Lectures on Artificial Intelligence & Machine Learning), Morgan & Claypool Publishers, 2010

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	1	-	-	-	2	2
CO2	1	-	2	2	2	2
CO3	1	-	2	2	2	2
CO4	1	-	2	2	2	2
CO5	1	-	2	2	2	2
CO	**1**	**-**	**2**	**2**	**2**	**2**

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: MATHEMATICAL BACKROUND	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: SUPERVISED LEARNING	2	1either or	2(2)-CO2	-	1either or (16)-CO5	-
Unit-III: UNSUPERVISED LEARNING	2	1either or	1(2)-CO3	1(2)-CO3	1either or (16)-CO5	-
Unit-IV: BAYESIAN	2	1either or	1(2)-CO4	1(2)-CO4	1either or	-

LEARNING					(16)-CO4	
Unit-V: NEURAL NETWORKS AND DEEP LEARNING	2	1either or	1(2)-CO5	1(2)-CO5 1either or (16)-CO5		-
Total Qns. Title:MX22203 MACHINE LEARNING TECHNIQUES	10	5either or	7(2)	3(2) 2 either or (16)	3 either or (16)	-
Total Marks	20	80	14	38	48	-
Weightage	20%	80%	14%	38%	32%	-

AE22313	**PCB DESIGN**	**L**	**T**	**P**	**C**
		3	**0**	**2**	**4**

COURSE OBJECTIVES:

- To understand the need for PCB Design and steps involved in PCB Design and Fabrication process
- To familiarize Schematic and layout design flow using Electronic Design Automation (EDA) Tools.
- To understand basic concepts of transmission line, crosstalk and thermal issues.
- To design (schematic and layout) PCB for analog circuits, digital circuits and mixed circuits
- Schematic creation & interpretation**.**

UNIT I	**INTRODUCTION TO PRINTED CIRCUIT BOARD**	**9**

Fundamental of electronic components, basic electronic circuits, Basics of printed circuit board designing: Layout planning, general rules and parameters, ground conductor considerations, thermal issues, check and inspection of artwork.

UNIT II	**DESIGN RULES FOR PCB**	**9**

Design rules for Digital circuit PCBs, Analog circuit PCBs, high frequency and fast pulse applications, Power electronic applications, Microwave applications,PCB Technology Trends: Multilayer PCBs. Multiwire PCB, Flexible PCBs, Surface mount PCBs, Reflow soldering, Introduction to High-Density Interconnection (HDI) Technology.

UNIT III	**INTRODUCTION TO ELECTRONIC DESIGN AUTOMATION(EDA) TOOLS FOR PCB DESIGNING**	**9**

Introduction to PCB Design using Distress tool, Introduction to PCB Design using Eagle tool, PCB Layout Designing, Auto routing and manual routing. Assigning specific text (silkscreen) to design, Creating report of design, creating manufacturing data (GERBER) for design.

UNIT IV	**INTRODUCTION PRINTED CIRCUIT BOARD PRODUCTION TECHNIQUES**	**9**

Photo printing, film-master production, reprographic camera, basic process for double sided PCBs photo resists, Screen printing process, plating, relative performance and quality control, Etching machines, Solders alloys, fluxes, soldering techniques, Mechanical operations

UNIT V	**PCB DESIGN FOR EMI/EMC**	**9**

Subsystem/PCB Placement in an enclosure, Filtering circuit placement, decoupling and bypassing, Electronic discharge protection, Electronic waste; Printed circuit boards Recycling techniques, Introduction to Integrated Circuit Packaging and footprints, NEMA and IPC standards.

TOTAL: 45 PERIODS

PRACTICAL EXERCISES: 30 PERIODS

LIST OF EXPERIMENTS	
1. Using any Electronic design automation (EDA) software, Practice following PCB Design steps(Open source EDA Tool KiCad Preferable or equivalent) Example circuit: Basic RC :Circuit Schematic Design: Familiarization of the Schematic Editor	
2. Schematic creation, Annotation using EDA tool for the given circuit.	
3. Netlist generation Layout Design: Familiarization of Footprint Editor	
4. Mapping of components, Creation of PCB layout Schematic.	
5. Create new schematic components and Create new component footprints.	
6. Design a single-sided PCB, mount the components and assemble in a cabinet for any one of the circuits mentioned below.	
TOTAL : 75 PERIODS	
COURSE OUTCOMES:	
At the end of the course, the students will be able to:	
CO1:	Appreciate the necessity, evolution, types and classes of PCB.
CO2:	Describe the steps involved in schematic, layout, fabrication and assembly process of PCB design.
CO3:	Explain advanced techniques, skills and modern tools for designing and fabrication of PCBs.
CO4:	Apply the knowledge and techniques to fabricate Multilayer, SMT and HDI PCB.
CO5:	Infer the trends in the design and fabrication of PCB.
REFERENCES:	
1.	Printed Circuits Handbook, Sixth Edition,by Clyde F.Coombs, Jr,HappyT. Holden, Publisher: McGraw-Hill Education Year: 2016
2.	Complete PCB Design Using OrCAD Capture and PCB Editor,Kraig Mitzner Bob Doe Alexander Akulin Anton Suponin Dirk Müller, 2nd Edition 2009.
3.	Introduction to System-on-Package, Rao R ,Tummala,&MadhavanSwaminathan, McGraw Hill, 2008
4.	Printed circuit board design ,fabrication assembly and testing By R. S. Khandpur, Tata McGraw Hill 2006
5.	EMC and Printed circuit board , Design theory and layout, Mark I Montrose IEEE compatibility society.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	1	2	2	2	2
CO2	2	1	2	2	2	2
CO3	2	1	2	2	2	2
CO4	2	1	2	2	2	2
CO5	2	1	2	2	2	2
CO	2	1	2	2	2	2

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: INTRODUCTION TO	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-

PRINTED CIRCUIT BOARD						
Unit-II: DESIGN RULES FOR PCB	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: INTRODUCTION TO ELECTRONIC DESIGN AUTOMATION(EDA) TOOLS FOR PCB DESIGNING	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: INTRODUCTION PRINTED CIRCUIT BOARD PRODUCTION TECHNIQUES	2	1either or	1(2)-CO4	1(2)-CO4	1either or (16)-CO4	-
Unit-V: PCB DESIGN FOR EMI/EMC	2	1either or	1(2)-CO5	1(2)-CO5 1either or (16)-CO5	-	-
Total Qns. Title AE22313 PCB DESIGN	10	5either or	7(2)	3(2) 4 either or (16)	1 either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

SEMESTER III, PROFESSIONAL ELECTIVE V

AE22321	**SENSORS AND ACTUATORS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- Understand static and dynamic characteristics of measurement systems.
- Study various types of sensors.
- Study different types of actuators and their usage.
- Study State-of-the-art digital and semiconductor sensors.

UNIT I	**INTRODUCTION TO MEASUREMENT SYSTEMS**	**9**

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance characteristics: static and dynamic characteristics of measurement systems, zero-order, first-order, and second-order measurement systems and response.

UNIT II	**RESISTIVE AND REACTIVE SENSORS**	**9**

Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & applicationto LVDT.

UNIT III	**SELF-GENERATING SENSORS**	**9**

Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors,

photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper and low-drift amplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers.		
UNIT IV	**ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS**	**9**
Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.		
UNIT V	**DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS**	**9**
Digital sensors: position encoders, variable frequency sensors — quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magnetotransistors, MOSFET transistors, CCD imaging sensors , ultrasonic sensors, fiber-optic sensors. Sensors for environmental monitoring.		
TOTAL: 45 PERIODS		

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Enumerate terminologies of measuring systems and sensor classifications
CO2:	Explain resistive and reactive sensors
CO3:	Discuss the signal conditioning and noise characteristics of self generating sensors actuators and its drive characteristics
CO4:	Explain sensors actuators and its drive characteristics
CO5:	Illustrate the applications of digital and semiconductor sensors

REFERENCES:

1.	Andrzej M.Pawlak, “Sensors and Actuators in Mechatronics Design and Applications ”, 2006.
2.	D.Johnson, “Process Control Instrumentation Technology”, John Wiley andSons, 8th Edition, 2014.
3.	D.Patranabis, “Sensors and Transducers”, TMH 2003.
4.	E.O.Doeblin, “Measurement System: Applications and Design”, McGraw Hill publications , 1996.
5.	Graham Brooker, “Introduction to Sensors for ranging and imaging”, Yesdee, 2009.
6.	Herman K.P. Neubrat, “Instrument Transducers – An Introduction to Their Performance andDesign”, Oxford University Press, 1999.
7.	Ian Sinclair, Sensors and Transducers, Elsevier, 3rd Edition, 2011.
8.	Jon Wilson, “Sensor Technology Handbook”, Newne, 2004.
9.	Kevin James, PC Interfacing and Data acquisition, Elsevier, 2011.
10.	Ramon PallásAreny, John G. Webster, “Sensors and Signal conditioning”, 2nd edition, JohnWiley and Sons, 2000.
11.	Sensors and Actuators: Control System Instrumentation, Clarence W. de Silva CRC Press,2007.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	-	2	1	-	2
CO2	2	-	2	1	-	2
CO3	2	-	2	1	-	2
CO4	2	-	2	1	-	2
CO5	2	-	2	1	-	2
CO	2	-	2	1	-	2

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: INTRODUCTION TO MEASUREMENT SYSTEMS	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: RESISTIVE AND REACTIVE SENSORS	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: SELF-GENERATING SENSORS	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS	2	1either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4	-	-
Unit-V: DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS	2	1either or	1(2)-CO5	1(2)-CO5 1either or (16)-CO5	-	-
Total Qns. Title: AE22321SENSORS AND ACTUATORS	10	5either or	7(2)	3(2) 5 either or (16)	-	-
Total Marks	20	80	14	86		-
Weightage	20%	80%	14%	86%		-

AE22322	DIGITAL HIGH SPEED DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To identify sources affecting the speed of digital circuits.
- To introduce methods to improve the signal transmission characteristics

UNIT I	SIGNAL PROPAGATION ON TRANSMISSION LINES	9

Transmission line equations, wave solution, wave vs. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching, input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNIT II	MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK	9

Multi-conductor transmission-lines, coupling physics, per unit length parameters, Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

UNIT III	NON-IDEAL EFFECTS	9

Non-ideal signal return paths – gaps, BGA fields, via transitions, Parasitic inductance and capacitance, Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

UNIT IV	POWER CONSIDERATIONS AND SYSTEM DESIGN	9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling , Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V	CLOCK DISTRIBUTION AND CLOCK OSCILLATORS	9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter, Applications of Clock Oscillator.

TOTAL:45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Define the sources affecting the speed of digital circuits.
CO2:	Identify methods to improve the signal transmission characteristics.
CO3:	Explain the non-ideal effects of signal.
CO4:	Compute the power consideration for the system.
CO5:	Estimate the clock distribution.

REFERENCES:

1.	H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, 1993.
2.	Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice Hall Modern Semiconductor Design,2012.
3.	S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.
4.	Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 2003.
5.	Stephen C. Thierauf, High-Speed Circuit Board Signal Integrity,Artech house Inc.,2004.

TOOLS REQUIRED

1.	SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2.	HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3.	SPECCTRAQUEST from Cadence, http://www.specctraquest.com

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	1	2	2	1
CO2	2	1	1	2	2	1
CO3	2	1	1	2	2	1
CO4	2	1	1	2	2	1
CO5	2	1	1	2	2	1
CO	2	1	1	2	2	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: SIGNAL PROPAGATION ON TRANSMISSION LINES	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: NON-IDEAL EFFECTS	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: POWER CONSIDERATIONS AND SYSTEM DESIGN	2	1either or	1(2)-CO4	1(2)-CO4	1either or (16)-CO4	-
Unit-V: CLOCK DISTRIBUTION AND CLOCK OSCILLATORS	2	1either or	1(2)-CO5	1(2)-CO5	1either or (16)-CO5	-
Total Qns. Title: AE22322 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN	10	5either or	7(2)	3(2) 3 either or (16)	2 either or (16)	-
Total Marks	20	80	14	54	32	-
Weightage	20%	80%	14%	54%	32%	-

AE22323	CONSUMER ELECTRONICS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To acquaint the students with the construction, theory and operation of the basic electronic devices and circuits.
- To know about the working principle of entertainment devices.
- To introduce the concept of Sensors and voice controls.
- To provide the knowledge on Smart home devices.
- To gain knowledge on current communication technology.

UNIT I	CONSUMER ELECTRONICS FUNDAMENTALS	9

History of Electronic Devices- Vacuum Tubes, Transistors, Integrated Circuits- Moore's Law, Semiconductor Devices, Diodes, Rectifiers, Transistors, Logic Gates, Combinational Circuits, ADC, DAC and Microprocessors, Microcontrollers in consumer electronics, Energy management, Intelligent Building Perspective. Wiring and Safety instructions.

UNIT II	ENTERTAINMENT ELECTRONICS	9

Audio systems: Construction and working principle of: Microphone, Loud speaker, AM and FM receiver, stereo, Home theatre. Display systems: CRT, LCD, LED and Graphics displays Video Players: DVD and Blue RAY. Recording Systems: Digital Cameras and Camcorders.

UNIT III	SMART HOME - SENSORS	9

Technology involved in Smart home, Home Virtual Assistants- Alexa and Google Home. Home Security Systems - Intruder Detection, Automated blinds, Motion Sensors, Thermal Sensors and Image Sensors, PIR, IR and Water Level Sensors.

UNIT IV	HOME APPLIANCES	9

Home Enablement Systems: RFID Home, Lighting control, Automatic Cleaning Robots, Washing Machines, Kitchen Electronics- Microwave, Dishwasher, Induction Stoves, Smart Refrigerators, Smart alarms, Smart toilet, Smart floor, Smart locks.

UNIT V	INTRODUCTION TO SMART OS AND COMMUNICATION	9

Introduction to Smart OS- Android and iOS. Video Conferencing Systems- Web/IP Camera, Video security, Internet Enabled Systems, Wi-Fi, IoT, Li-Fi, GPS and Tracking Systems. Cordless Telephones, Fax Machines, PDAs- Tablets, Smart Phones and Smart Watches.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Infer the various electronic components used for designing electronic gadgets.
CO2:	Demonstrate the concepts behind the entertainment gadgets.
CO3:	Identify the supporting sensors used for automation.
CO4:	Interpret various home appliances.
CO5:	Apply advance techniques, skills and modern tools on home applications.

REFERENCES:

1	Thomas L Floyd "Electronic Devices" 10th Edition Pearson Education Asia 2018.
2	Nick vandome, Smart homes in easy steps, - Master smart technology for your home 2018.
3	Jordan Frith, " Smartphones as Locative Media ", Wiley. 2014.
4	Dennis C Brewer, " Home Automation", Que Publishing 2013.
5	Thomas M. Coughlin, "Digital Storage in Consumer Electronics", Elsevier and Newness 2012.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	1	2	2	2	2
CO2	2	1	2	2	2	2
CO3	2	1	2	2	2	2
CO4	2	1	2	2	2	2
CO5	2	1	2	2	2	2
CO	2	1	2	2	2	2

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: CONSUMER ELECTRONICS FUNDAMENTALS	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: ENTERTAINMENT ELECTRONICS	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: SMART HOME - SENSORS	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: HOME APPLIANCES	2	1either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4	-	-
Unit-V: INTRODUCTION TO SMART OS AND COMMUNICATION	2	1either or	1(2)-CO5	1(2)-CO5	1either or (16)-CO5	-
Total Qns. Title:AE22323 CONSUMER ELECTRONICS	10	5either or	7(2)	3(2) 4 either or (16)	1either or (16)	-
Total Marks	20	80	14	70	16	-
Weightage	20%	80%	14%	70%	16%	-

AE22324	**ADVANCED MICROPROCESSORS AND MICROCONTROLLERS ARCHITECTURE**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To expose the students to the fundamentals of microprocessor architecture.
- To explore the high performance features in CISC architecture.
- To familiarize the high performance features in RISC architecture.

• To introduce the basic features in Motorola microcontrollers.		
• To enable the students to understand PIC Microcontroller.		
UNIT I	**MICROPROCESSOR ARCHITECTURE**	**9**
Instruction Set – Addressing modes – Memory hierarchy –register file – Cache – Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards–instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.		
UNIT II	**HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM**	**9**
CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.		
UNIT III	**HIGH PERFORMANCE RISC ARCHITECTURE – ARM**	**9**
Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.		
UNIT IV	**MSP430 16 - BIT MICROCONTROLLER**	**9**
The MSP430 Architecture- CPU Registers - Instruction Set, On-Chip Peripherals - MSP430 - Development Tools, ADC - PWM - UART - Timer Interrupts - System design using MSP430Microcontroller.		
UNIT V	**PIC MICROCONTROLLER**	**9**
CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter.		
		TOTAL: 45 PERIODS
COURSE OUTCOMES:		
At the end of the course, the students will be able to:		
CO1:	Explain the fundamentals of microprocessor architecture.	
CO2:	Identify the high performance features in CISC architecture.	
CO3:	Choose the high performance features in RISC architecture.	
CO4:	Organize the basic features in Motorola microcontrollers.	
CO5:	Develope PIC Microcontroller for Interfacing.	
REFERENCES:		

1.	Daniel Tabak , " Advanced Microprocessors", McGraw Hill.Inc., 1995
2.	Parimala Devi, P. Jayachandar P and Brindha," Advanced Microprocessors and Microcontrollers", Laxmi Publications Pvt Ltd.,2019.
3.	Ramesh Gaonkar, "Microprocessor Architecture, Programming and Applications with the 8085",6th Edition,2013.
4.	Steve Heath," Microprocessor Architectures and Systems: RISC, CISC and DSP", Elsevier Science , 2014.
5.	James L. Antonakos , " The Pentium Microprocessor", Pearson Education , 1997.
6.	Joseph Yiu ,"System-on-Chip Design with Arm® Cortex®-M Processors",arm Education Media, 2019.
7.	Steve Furber , " ARM System –On –Chip architecture", Addision Wesley , 2000.
8.	Gene .H.Miller ," Micro Computer Engineering ", Pearson Education , 2003.
9.	John .B.Peatman , " Design with PIC Microcontroller" , Prentice hall, 1997.
10.	John H.Davis , "MSP 430 Micro controller basics", Eelsevier, 2008.
11.	James L.Antonakos, "An Introduction to the Intel family of Microprocessors", Pearson Education 1999.
12.	Barry.B.Breg," The Intel Microprocessors Architecture, Programming and Interfacing ", PHI,2002.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	-	2	2	2	1
CO2	2	-	2	2	2	1
CO3	2	-	2	2	2	1
CO4	2	-	2	2	2	1
CO5	2	-	2	2	2	1
CO	2	-	2	2	2	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: MICROPROCESSOR ARCHITECTURE	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II:HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: HIGH PERFORMANCE RISC ARCHITECTURE – ARM	2	1either or	1(2)-CO3	1(2)-CO3	-1either or (16)-CO3	-
Unit-IV: MSP430 16 - BIT MICROCONTROLLER	2	1either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4		-
Unit-V: PIC MICROCONTROLLER	2	1either or	1(2)-CO5	1(2)-CO5	1either or (16)-CO5	-
Total Qns. Title ADVANCED MICROPROCESSORS& MICROCONTROLLERS ARCHITECTURE	10	5either or	7(2)	3(2) 3 either or (16)	2 either or (16)	-
Total Marks	20	80	14	54	32	-
Weightage	20%	80%	14%	54%	32%	-

AE22325	**AUTOMOTIVE ELECTRONICS**	**L**	**T**	**P**	**C**
		3	**0**	**0**	**3**

COURSE OBJECTIVES:

- To explain the principle of electronic management system and different sensors used in the systems.
- To know the concepts and develop basic skills necessary to diagnose automotive electronic problems.
- To know Starting, and charging, lighting systems, advanced automotive electrical

systems.

- To include electronic accessories and basic computer control.
- To explore practically about the components present in an Automotive electrical and electronics system.

UNIT I	FUNDAMENTALS	9

Components for electronic engine management system, open and closed loop control strategies, PID control, Look up tables, introduction to modern control strategies like Fuzzy logic and adaptive control. Switches, active resistors, Transistors, Current mirrors/amplifiers, Voltage and current references, Comparator, Multiplier. Amplifier, filters, A/D and D/A converters.

UNIT II	MODERN SENSORS	9

Film sensors, micro-scale sensors, Particle measuring systems, Vibration Sensors, SMART sensors, Machine Vision, Multi-sensor systems Applications of Sensors: Applications and case studies of Sensors in Automobile Engineering, Aeronautics, Machine tools and Manufacturing processes.

UNIT III	CHARGING SYSTEM	9

Generation of Direct Current- Shunt Generator Characteristics- Armature Reaction- Third Brush Regulation- Cutout. Voltage and Current Regulators- Compensated Voltage Regulator Alternators Principle and Constructional Aspects and Bridge Rectifiers- New Developments.

UNIT IV	AUTOMOTIVE TRANSMISSION CONTROL SYSTEMS	9

Transmission control - Cruise control – Braking control – Traction control –Suspension control –Steering control – Stability control – Integrated engine control.

UNIT V	ELECTRONICS SYSTEMS	9

Current Trends in Automotive Electronic Engine Management System- Types of EMS Electromagnetic interference Suppression- Electromagnetic Compatibility- Electronic Dashboard Instruments- Onboard Diagnostic System- Security - Warning System infotainment and Telematics. Case study: Automotive stepper motor.

TOTAL: 45 PERIODS

SUGGESTED ACTIVITIES:

1. Testing of battery, starting systems, charging systems, ignition systems and body controller systems.
2. Study of various sensors and actuators used in two wheelers and four wheelers for electronic control.
3. Study of Development of Embedded Systems projects.

COURSE OUTCOMES:

At the end of the course, the students will be able to:

CO1:	Explain the fundamentals of electronic engine management system.
CO2:	Illustrate the functions of various modern sensors in engine management systems.
CO3:	Demonstrate charging system and advanced automotive electrical systems.
CO4:	Summarize the automotive transmission control systems.
CO5:	Explain the components present in an Automotive electronics system.

REFERENCES:

1.	Allan Bonnick, “Automotive Computer Controlled Systems”, Butterworth- Heinemann, Elsev Indian Edition, 2011.
2.	A. Galip Ulsoy, Huei Peng, Melih Cakmakci, “Automative Control Systems”, Cambridge University Press, 2012.
3.	Akkadiusz Gola, “Design and Management of Manufacturing Systems, MDPI, 2021.
4.	Tom Denton, “Automobile Electrical and Electronic Systems, 5th Edition, Routledge, 2018.
5.	William B Ribbens, “Understanding automotive electronics”, 5th edition - Butter worth Hein Woburn, 1998.

Mapping of Course Outcomes to Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	-	2	1	-	1
CO2	2	-	2	1	-	1
CO3	2	-	2	1	-	1
CO4	2	-	2	1	-	1
CO5	2	-	2	1	-	1
CO	2	-	2	1	-	1

Table of Specification for End Semester Question Paper

Unit No. and Title	Total 2 Marks Qus.	Total 16 Marks Qus.	Cognitive Level			
			Remember (Kn)	Understand (Un)	Apply (Ap)	Analyse(An) Evaluate(Ev)
Unit-I: FUNDAMENTALS	2	1either or	2(2)-CO1	1either or (16)-CO1	-	-
Unit-II: MODERN SENSORS	2	1either or	2(2)-CO2	1either or (16)-CO2	-	-
Unit-III: CHARGING SYSTEM	2	1either or	1(2)-CO3	1(2)-CO3 1either or (16)-CO3	-	-
Unit-IV: AUTOMOTIVE TRANSMISSION CONTROL SYSTEMS	2	1either or	1(2)-CO4	1(2)-CO4 1either or (16)-CO4	-	-
Unit-V: ELECTRONICS SYSTEMS	2	1either or	2(2)-CO5	1either or (16)-CO5	-	-
Total Qns. Title:AE22325 AUTOMOTIVE ELECTRONICS	10	5either or	8(2)	2(2) 5 either or (16)	-	-
Total Marks	20	80	16	84		-
Weightage	20%	80%	14%	84%		-

AUDIT COURSES

AC22101	**ENGLISH FOR RESEARCH PAPER WRITING**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**
COURSE OBJECTIVES:					
• Teach how to improve writing skills and level of readability					
• Tell about what to write in each section					
• Summarize the skills needed when writing a Title					
• Infer the skills needed when writing the Conclusion					
• Ensure the quality of paper at very first-time submission					
UNIT I	**INTRODUCTION TO RESEARCH PAPER WRITING**				**6**
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and					

Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.		
UNIT II	**PRESENTATION SKILLS**	**6**
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction.		
UNIT III	**TITLE WRITING SKILLS**	**6**
Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.		
UNIT IV	**RESULT WRITING SKILLS**	**6**
Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions.		
UNIT V	**VERIFICATION SKILLS**	**6**
Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission.		
		TOTAL: 30 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will.../ will be able to...	
CO1:	Understand that how to improve your writing skills and level of readability
CO2:	Learn about what to write in each section
CO3:	Understand the skills needed when writing a title
CO4:	Understand the skills needed when writing the conclusion
CO5:	Ensure the good quality of paper at very first-time submission
REFERENCES:	
1	Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.
2	Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006.
3	Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.

Mapping of Course Outcomes with Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	-	2	-	1	-	-
CO2	-	2	-	1	-	-
CO3	-	2	-	1	-	-
CO4	-	2	-	1	-	-
CO5	-	2	-	1	-	-
CO	-	2	-	1	-	-

AC22102	**CONSTITUTION OF INDIA**	**L**	**T**	**P**	**C**
		2	**0**	**0**	**0**
COURSE OBJECTIVES:					
• Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective					
• To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism					

• To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution		
UNIT I	**HISTORY OF MAKING OF THE INDIAN CONSTITUTION**	**5**
History, Drafting Committee, (Composition & Working).		
UNIT II	**PHILOSOPHY OF THE INDIAN CONSTITUTION**	**5**
Preamble, Salient Features		
UNIT III	**CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES**	**5**
Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.		
UNIT IV	**ORGANS OF GOVERNANCE**	**5**
Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.		
UNIT V	**LOCAL ADMINISTRATION**	**5**
District's Administration head: Role and Importance Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: ZilaPachayat. Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.		
UNIT VI	**ELECTION COMMISSION**	5
Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.		
		TOTAL: 30 PERIODS

COURSE OUTCOMES:	
Upon completion of the course, the students will.../ will be able to...	
CO1:	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics
CO2:	Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India
CO3:	Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution
CO4:	Discuss the passage of the Hindu Code Bill of 1956.

REFERENCES:	
1	The Constitution of India, 1950 (Bare Act),Government Publication.
2	Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3	M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4	D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Mapping of Course Outcomes with Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	-	2	1	-	-	-
CO2	-	2	1	-	-	-
CO3	-	2	1	-	-	-
CO4	-	2	1	-	-	-
CO5	-	2	1	-	-	-
CO	-	2	1	-	-	-

AC22201	DISASTER MANAGEMENT	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES:

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations
- Develop the strengths and weaknesses of disaster management approaches

UNIT I	INTRODUCTION	6

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II	REPERCUSSIONS OF DISASTERS AND HAZARDS	6

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III	DISASTER PRONE AREAS IN INDIA	6

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics.

UNIT IV	DISASTER PREPAREDNESS AND MANAGEMENT	6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V	RISK ASSESSMENT	6

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

Upon completion of the course, the students will.../ will be able to...

CO1:	Summarize basics of disaster
CO2:	Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response
CO3:	Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives
CO4:	Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations
CO5:	Develop the strengths and weaknesses of disaster management approaches

REFERENCES:

1	Goel S. L., Disaster Administration And Management Text And Case Studies",Deep &Deep Publication Pvt. Ltd., New Delhi,2009.
2	Nishitha Rai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies" New Royal book Company, 2007.
3	Sahni, Pardeep Et.al, "Disaster Mitigation Experiences And Reflections", Prentice Hall of India, New Delhi, 2001.

Mapping of Course Outcomes with Programme Outcomes

Course Outcomes	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	-	-	-	1	2
CO2	1	-	-	-	1	2
CO3	1	-	-	-	1	2
CO4	1	-	-	-	1	2
CO5	1	-	-	-	1	2
CO	1	-	-	-	1	2

AC22202	நற்றமிழ் இலக்கியம்	L	T	P	C
		2	0	0	0
UNIT I	சங்க இலக்கியம்				6
1. தமிழின் துவக்க நூல் தொல்காப்பியம் - எழுத்து, சொல், பொருள் 2. அகநானூறு (82) - இயற்கை இன்னிசை அரங்கம் 3. குறிஞ்சிப் பாட்டின் மலர்க்காட்சி 4. புறநானூறு (95,195) - போரை நிறுத்திய ஔவையார்					
UNIT II	அறநெறித் தமிழ்				6
1. அறநெறி வகுத்த திருவள்ளுவர் - அறம் வலியுறுத்தல், அன்புடைமை, ஒப்புரவறிதல், ஈகை, புகழ் 2. பிற அறநூல்கள் - இலக்கிய மருந்து - ஏலாதி, சிறுபஞ்சமூலம், திரிகடுகம், ஆசாரக்கோவை (தூய்மையை வலியுறுத்தும் நூல்)					
UNIT III	இரட்டைக் காப்பியங்கள்				6
1. கண்ணகியின் புரட்சி - சிலப்பதிகார வழக்குரை காதை 2. சமூகசேவை இலக்கியம் மணிமேகலை - சிறைக்கோட்டம் அறக்கோட்டமாகிய காதை					
UNIT IV	அருள்நெறித் தமிழ்				6
1. சிறுபாணாற்றுப்படை - பாரி முல்லைக்குத் தேர் கொடுத்தது, பேகன் மயிலுக்குப் போர்வை கொடுத்தது, அதியமான் ஔவைக்கு நெல்லிக்கனி கொடுத்தது, அரசர் பண்புகள் 2. நற்றிணை - அன்னைக்குரிய புன்னை சிறப்பு 3. திருமந்திரம் (617, 618) - இயமம் நியமம் விதிகள் 4. தர்மச்சாலையை நிறுவிய வள்ளலார் 5. புறநானூறு - சிறுவனே வள்ளலானான் 6. அகநானூறு (4) - வண்டு நற்றிணை (11) - நண்டு கலித்தொகை (11) - யானை, புறா ஐந்திணை 50 (27) - மான் ஆகியவை பற்றிய செய்திகள்					
UNIT V	நவீன தமிழ் இலக்கியம்				6
1.உரைநடைத் தமிழ், - தமிழின் முதல் புதினம், - தமிழின் முதல் சிறுகதை, - கட்டுரை இலக்கியம்,					

- பயண இலக்கியம், - நாடகம், 2.நாட்டு விடுதலை போராட்டமும் தமிழ் இலக்கியமும், 3. சமுதாய விடுதலையும் தமிழ் இலக்கியமும், 4.பெண் விடுதலையும் விளிம்பு நிலையினரின் மேம்பாட்டில் தமிழ் இலக்கியமும், 5.அறிவியல் தமிழ், 6.இணையத்தில் தமிழ், 7.சுற்றுச்சூழல் மேம்பாட்டில் தமிழ் இலக்கியம்.	
TOTAL: 30 PERIODS	
REFERENCES:	
1	தமிழ் இணைய கல்விக்கழகம் (Tamil Virtual University)
2	தமிழ் விக்கிப்பீடியா (Tamil Wikipedia)
3	தர்மபுர ஆதீன வெளியீடு
4	வாழ்வியல் களஞ்சியம்
5	தமிழ்கலைக் களஞ்சியம் - தமிழ் வளர்ச்சித் துறை (thamilvalarchithurai.com)
6	அறிவியல் களஞ்சியம் - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்